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ABSTRACT

The Producer Price Index (PPI) for the United States suggests that semiconductor prices have barely been falling in recent years, a dramatic contrast from the rapid declines reported from the mid-1980s to the early 2000s. This slowdown in the rate of decline is puzzling in light of evidence that the performance of microprocessor units (MPUs) has continued to improve at a rapid pace. Roughly coincident with the shift to slower price declines in the PPI, Intel — the leading producer of MPUs — substantially changed its pricing behavior for these chips. As a result of this change, we argue that the matched-model methodology used in the PPI for MPUs likely started to be biased in the mid-2000s and that hedonic indexes can provide a more accurate measure of price change since then. Our preferred hedonic index of MPU prices tracks the PPI closely through 2004. However, from 2004 to 2008, our preferred index fell faster than the PPI, and from 2008 to 2013 the gap widened further, with our preferred index falling at an average annual rate of 43 percent, while the PPI declined at only an 8 percent rate. Given that MPUs currently represent about half of U.S. shipments of semiconductors, this difference has important implications for gauging the rate of innovation in the semiconductor sector.

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1. Introduction

How fast are semiconductor prices falling? Data from the Producer Price Index (PPI) published by the U.S. Bureau of Labor Statistics indicate that prices of microprocessor units (MPUs) have barely been falling in recent years. This very slow rate of price decline stands in sharp contrast to the rapid declines in MPU prices reported from the mid-1980s up to the early 2000s and the exceptionally rapid declines in the latter half of the 1990s. If accurate, the apparent slowdown in MPU price declines in recent years would be troubling, given the long-run relationship between rates of price decline of semiconductors and the pace of innovation in that sector.[1]

A stalling out of innovation in this sector likely would have broader implications for the economy, as semiconductors are an important general-purpose technology lying behind advances of the digital revolution, including machine learning, robotics, big data, and massive connectivity.[2] Given this connection, adverse developments in the semiconductor sector could damp the growth potential of the overall economy.[3] On the other hand, if technological progress and attendant price declines were to continue at a rapid pace, powerful incentives would be in place for continued development and diffusion of new applications of this general-purpose technology. Such applications could both enhance the economy's growth potential and push forward the ongoing automation that has generated concerns about job displacement.[4]

The apparent slowdown in the rate of price decline is puzzling given evidence that the performance of MPUs continued to improve at a rapid pace after the mid-2000s. The key to resolving the puzzle may reside in another development in the semiconductor industry. Roughly

[1] See Aizcorbe, Oliner, and Sichel (2008) for a discussion of the relationship between price change and innovation for semiconductors.
[2] Brynjolfsson and McAfee (2014) and Baily, Manyika, and Gupta (2013) highlight key innovations in many sectors of the economy.
[3] For discussions of the sources of a possible slowdown in the economy's potential growth rate, see Cowen (2011), Fernald (2014), Gordon (2012, 2014a, and 2014b), Hall (2014), and Jorgenson, Ho, and Samuels (2014).
[4] For a recent discussion of these employment issues, see Hamilton Project (2015) for the transcript of a wide-ranging Policy Forum.

coincident with the shift to a slower pace of price decline in the PPI, Intel — the leading MPU producer — dramatically changed its pricing behavior. Prior to the mid-2000s, Intel generally lowered the list prices of existing chips to remain competitive with newly-introduced chips on a price-performance basis. However, after the mid-2000s, Intel shifted to a new paradigm in which it largely kept the list prices of existing chips unchanged.

This change in Intel's behavior could resolve the puzzling disconnect between continuing improvements in MPU performance and the shift to slower price declines. Namely, we argue that the matched-model methodology used by BLS is not well suited to capturing price trends in a pricing regime like the one that has prevailed since the mid-2000s. In such a pricing regime, if performance is improving over time, then matched-model price indexes for MPUs such as the PPI likely are biased. We argue that a specific hedonic index — one based on prices for newly-introduced models — is better suited to capturing price trends in these circumstances and develop new hedonic indexes for quality-adjusted prices using price data for Intel MPUs from 2000 to 2013.

Our preferred index of MPU prices tracks the PPI closely from 2000 to 2004. However, from 2004 to 2008 — roughly the period of transition to Intel's new pricing regime — our preferred index fell faster than the PPI. And from 2008 to 2013, the gap widened further, with our preferred index falling at an average annual rate of 43 percent, while the PPI declined at only an 8 percent rate.

An important innovation in the paper is that the hedonic regressions utilize measures of MPU performance on typical tasks for computer users rather than technical variables capturing physical characteristics (such as feature size) and engineering specifications (such as clock speed). Performance measures provide a superior control for quality change when constructing

price indexes for MPUs because they gauge the actual output obtained by a user rather than the input characteristics used to produce that output. Moreover, with rapid changes in MPU architecture in recent years, identifying the correct set of technical characteristics (and likely changes in that set) could be challenging.

To gauge whether our measure of user performance matters empirically, we also estimate parallel hedonic regressions with technical characteristics as the controls for chip quality. The price indexes generated by the two approaches are strikingly different after 2004. The declines in the indexes based on technical characteristics slowed sharply from that point forward, much like the PPI. After 2004, clock speed — which had been highly correlated with user performance — stopped rising in response to problems with heat generation, but Intel continued to boost performance in other ways. The hedonic regressions we estimated with technical characteristics evidently cannot capture the ongoing gains in performance, which translates into slower declines in constant-quality prices. This result highlights the importance of using direct measures of performance when estimating hedonic price regressions.

This paper focuses on MPUs rather than a broader set of semiconductor products, a choice we made for several reasons.[5] First, MPUs are a large segment of the semiconductor sector; in 2014, they represented about half of U.S. shipments (the scope of the PPI). Second, price series for MPUs extend back to the mid-1980s, allowing for comparisons of price trends over time. Given that price trends in this sector often are used to infer rates of technical progress, this historical comparability is important. Finally, we believe that developments in

[5] Among all MPUs, this paper analyzes prices of the MPUs used in desktop personal computers (PCs), for which data are the most readily available. In other work, we are developing indexes for MPUs going into servers, the types of machines that would support cloud computing in server farms and other processor-intensive applications. In addition, Dan Sichel's undergraduate thesis student, Sophie (Liyang) Sun (2014) developed price indexes for MPUs used in laptop computers.

MPU technology likely provide a rough guide to developments in other parts of the semiconductor sector, such as the chips that are used in smartphones and tablets.[6]

Our work on MPU prices builds on important earlier research. Much prior work on semiconductor prices relied on technical characteristics of the chips to control for quality. Notable studies that have used this approach to construct hedonic price indexes for semiconductors (or computing equipment that embeds these chips) include Cole et al. (1986), Grimm (1998), and Flamm (2007).

Although the technical characteristics used in these studies are correlated with performance, they may not fully capture the capabilities of the processor for end users. For this reason, Triplett (1989) and Berndt and Griliches (1993) called for analysis of computer prices with controls for more refined measures of performance.[7] In this vein, Chwelos (2000 and 2003) constructed hedonic price indexes for PCs with controls for the results of a suite of benchmark performance tests.[8]

An alternative approach has been to measure semiconductor prices with matched-model indexes. Aizcorbe, Corrado, and Doms (2003) found that under certain circumstances (highly granular data on model prices and high-frequency observations), a matched-model index may produce similar results to a hedonic index. Such highly granular data were used by the Federal Reserve Board for its MPU price index through 2006, which was constructed as a matched-model index. The source data used by the Fed were discontinued after 2006. However, even if

[6] The market for chips going into smartphones and tablets is changing rapidly, and it is challenging to obtain consistent time series on prices and performance. That being said, the production processes and technologies are similar enough to those for MPUs that developments in MPUs likely provide at least a rough gauge of developments in these other types of chips.

[7] See pages 147 and 91, respectively.

[8] In addition, Holdway (2001) examined unit value MPU price indexes using benchmark test scores as a measure of quality-adjusted units of computing power. Grimm (1998) developed specifications that controlled for millions of instructions per second (MIPS); this measure of performance, however, has limited ability to account for differences across MPUs in the translation of instructions into program execution.

those data were still available, the issues explored in this paper suggest that the matched-model approach would be problematic for more recent years.

This paper extends the existing literature in two main ways. First, we develop hedonic price indexes for MPUs that control for quality with performance measures based on typical tasks performed by end users. Second, we use these hedonic price indexes to assess the possibility that the PPI has been understating the price declines for MPUs.

The next section highlights the puzzle raised by the very slow rate of decline in the PPI during recent years at the same time that the engineering frontier for MPUs continued to move out rapidly. This section also discusses the change in the pricing pattern of Intel MPUs that occurred in the mid-2000s. Section 3 presents our argument that hedonic price indexes are likely to better capture price trends than are matched-model indexes (such as the PPI) since that change. Section 4 reviews our data, which cover the period from 2000 to 2013. In section 5, we describe the hedonic regressions used to obtain measures of quality-adjusted prices. Section 6 presents our results, and section 7 concludes.

2. The Puzzle

As noted, the PPI for MPUs has fallen very slowly in recent years. This section explores the plausibility of this extreme slowdown from two different perspectives. The first perspective is whether the slowdown meshes with the trends in technological advance for MPU chips. The second perspective focuses on the changes that occurred in Intel's pricing patterns for MPUs, developments that, as we show below, have important implications for price index measurement.

Technology cycles and chip performance.[9] The standard definition of a semiconductor technology cycle is the amount of time required to achieve a 30 percent reduction in the width of the smallest feature on a chip. Because chips are rectangular, a 30 percent reduction in both the horizontal and vertical directions implies about a 50 percent reduction (0.7*0.7) in the area required for the smallest chip component. As documented in Byrne, Oliner, and Sichel (2013), the semiconductor industry has achieved massive reductions in scaling over time. Indeed, the area occupied by a chip component in 2012 was roughly 200,000 times smaller than in 1969.

There is a broad consensus that the pace of technical advance in the semiconductor industry sped up in the mid-1990s, a development first brought to the attention of economists by Jorgenson (2001). Table 1 reports the average length of the semiconductor technology cycle (as defined above) for various periods. For the industry as a whole, the technology cycle averaged three years until 1993 and then dropped to about two years from 1993 to 2012. Within the later period, the scaling advances were especially rapid from 1993 to 2003 and a bit slower after 2003. Even so, the average cycle since 2003 has remained substantially shorter than the three-year cycle in effect before the 1990s. For Intel's MPU chips, there has been no pullback at all from the two-year cycle. The upshot is that the cycles in semiconductor technology — a key driver of quality improvement in IT products — have remained rapid.[10]

While the pace of miniaturization has been sustained, semiconductor producers have changed the approach used to translate these engineering gains into faster performance. Historically, each new generation of technology in semiconductors allowed for an increase in the

[9] The text in this section draws heavily on material in Byrne, Oliner, and Sichel (2013). In addition, table 1 comes directly from that paper.

[10] These continuous increases in chip density are the force behind Moore's Law, which states that the number of components on leading-edge chips will double every two years. Moore's original formulation (Moore, 1965) pegged the doubling time at only one year, but in 1975 he revised the period to be two years based on the actual experience to that point (Intel Corporation, 2005). For a discussion of the outlook for Moore's Law, see Bauer, Veira, and Weig (2013).

number of basic calculations performed per second (clock speed) for a given chip design. However, as speed continued to increase, dissipating the generated heat became problematic. In response, Intel shifted away in the early to mid-2000s from increases in clock speed and boosted performance instead by placing multiple copies of the core architecture on each chip — a change enabled by smaller feature size — and by improving the design of those cores.[11]

How did this strategy shift affect the rate of increase in performance for end users? For the period through 2008, Pillai (2013) addressed this question with performance scores from the Standard Performance Evaluation Corporation (SPEC).[12] These scores are based on standard tasks designed to reflect the needs of computer users. Figure 1 extends Pillai's analysis through 2013, plotting average SPEC performance measures for MPUs introduced each year.[13] Starting in 2004, the figure includes a second SPEC performance measure (the "rate" score) that incorporates more fully the performance gain from using multiple cores than does the standard ("speed") measure.[14]

Figure 1 confirms Pillai's finding that MPU performance gains cooled around 2001 from the extraordinary pace in the 1990s, though the rate of advance has, nonetheless, remained substantial through 2013. Using the SPEC rate measure that accounts more completely for the effects of parallel processing, SPEC performance rose about 32 percent per year on average from 2000 to 2013, down from the 60 percent rate of improvement from 1990 to 2000 and the 36 percent pace over the earlier 1971-90 period (not shown). The figure also plots clock speed for

[11] See Shenoy and Daniel (2006). Also, Hennessy and Patterson (2012) document that increases in clock speed stalled out during this period (figure 1.11, p. 24).
[12] SPEC is a non-profit corporation that establishes performance benchmark tests for computing equipment and publishes test results submitted by member organizations.
[13] The data through 1999 were kindly provided by Unni Pillai. We linked these data with SPEC performance results for 1999-2013 that we obtained directly from SPEC. We accessed the SPEC data on May 20, 2014 and used the benchmark suites SPEC® CPU2006 and SPEC® CPU2000. The SPEC score for each year is the average over the Intel desktop MPU chips introduced in that year. Details are provided in section 4 and in appendix A.
[14] See section 4 for further discussion of these alternative SPEC tests.

Intel desktop MPUs, highlighting that performance continued to improve even as clock speed stalled out in the early to mid-2000s.[15]

Historically, improvements in the engineering frontier have translated into steep declines in MPU prices. Figure 2 shows the annual price declines back to 1986, splicing together estimates from Grimm (1998) through 1992, the Federal Reserve Board for 1993-97, and the PPI for later years. Over this period, MPU prices fell at an average rate of nearly 30 percent per year, with especially sharp drops in the second half of the 1990s. However, reported price declines have slowed dramatically over the past several years. Indeed, the declines in each year since 2010 were smaller than in any prior year back to 1986, breaking the link with the continued engineering improvements. Perhaps the cost of achieving these engineering advances has accelerated in recent years. If that were the case, we might expect to see a similar price pattern for other types of semiconductor chips. No such pattern, though, is evident for memory chips (DRAMs).[16] As shown in figure 3, DRAM prices have been quite volatile from year to year, with no clear trend toward slower declines. At least for DRAMs, then, the translation of the engineering frontier to prices does not appear to have changed.

All in all, the shift to much slower price declines for microprocessors in the PPI is a puzzle in light of the continued substantial improvements on the engineering front. We next consider the possibility that changes in the properties of Intel's posted prices after 2006 could have distorted the measurement of price trends in the PPI.

[15] During the first half of the 1990s, performance also increased more rapidly than did clock speed. Hennessy and Patterson (2012) discuss this pattern; see the note to their figure 1.11.

[16] The most important driver of DRAM performance is the size of the components on the chip, which has continued to shrink rapidly, as discussed above. See Flamm (1993) for a discussion of characteristics of DRAM chips.

Intel's pricing behavior and market position. Between 2003 and 2006, the properties of Intel's posted prices for MPU chips changed dramatically.[17] Prior to 2003, the price of a specific Intel MPU model tended to drop fairly rapidly in the year or two following its introduction, especially once a new, higher performance model became available. By 2006, this pattern had completely changed; the posted price of a specific model tended to remain constant, even after a new, higher performance model became available at a similar price.

Figure 4 illustrates this shift in pricing behavior. The upper panel shows Intel wholesale list prices for all desktop models during 2000-01, while the lower panel shows the analogous list prices for all desktop models during 2011-12. The difference between the two panels is stark. In the early period, prices fell steeply over a model's lifecycle. However, by 2011-12, the price paths are flat or nearly so, with only a few instances of sizable price declines. Figure 5 summarizes this change in life-cycle pricing over the entire 2000-12 period by showing the share of all Intel desktop MPU models introduced in each year that experienced a price decline within four quarters of introduction.[18] As can be seen, every model introduced in 2000 and 2001 had at least one such price cut. But the share then dropped to about 60 percent for the 2004 to 2009 cohorts and took another leg down thereafter, falling to roughly 10 percent for the 2012 cohort.

This shift took place against the backdrop of a changing competitive environment vis-a-vis AMD, Intel's primary challenger in the MPU market. Figure 6 plots Intel's annual revenue from all products (not only MPUs) as a share of Intel's and AMD's combined revenue. Over this 20-year period, Intel's revenue share ranged from just under 80 percent to slightly above 90 percent. In 2002 and 2003, Intel's share stood at the top of this range but then eroded

[17] While the BLS does not indicate which companies' prices are included in the PPI for MPUs, it is only reasonable to assume that Intel is included given its dominant market position. Moreover, it appears that BLS has been making at least some use of Intel's posted prices for MPUs (see Holdway, 2001).
[18] The price data in the figure are described in section 4.

significantly through 2006. Nosko (2010) also documented this share erosion, noting that from 2002 to 2006, AMD "consistently released products whose price/performance characteristics were similar to or beat Intel's" (p. 8). Documents from legal actions against Intel for alleged antitrust violations (see, for example, State of New York v. Intel Corporation, 2009) also provide evidence that Intel was concerned about its losses of market share to AMD during this period.

However, in 2006, Intel began to turn the corner by offering new MPUs that dominated those sold by AMD (see Nosko, 2010, for details) and subsequently pulled ahead of AMD in a decisive way, consistent with the recovery in Intel's overall revenue share. By 2013, Intel's dominance had reached the point that AMD effectively had been relegated to the bottom end of the MPU market. Indeed, as shown in figure 7, AMD received more than 85 percent of its MPU revenue from chips that sold for less than $75, the low-end part of the market where Intel derived only about 15 percent of its revenue. Conversely, Intel received almost 30 percent of its MPU revenue from chips that sold for $200 or more, a segment in which AMD earned no revenue.[19]

This evidence indicates that Intel has enhanced its position in the MPU market since 2006. With less competition from AMD, Intel has greater scope to manage its price structure.[20] By keeping list prices essentially fixed over a chip's life cycle, Intel may be attempting to extract more revenue from price-insensitive buyers while offering discounts on a case-by-case basis to other customers. Such price discrimination could reduce the information content of its posted list prices, potentially biasing the quality-adjusted indexes generated from these prices. The next

[19] Figure 7 slightly overstates the market separation between Intel and AMD for the following reason. The source data used to construct the figure show the average selling prices for distinct product families (Intel's Core i5 Duo, for example) rather than prices for individual chips. Within each product family, there is some amount of unobserved price variation. The average selling price for AMD's most expensive product family, the FX-8, was less than $200 in 2013, but two chips in this family (the FX-9590 and the FX-9370) were priced between $200 and $500 at introduction in July 2013 (see http://en.wikipedia.org/wiki/List_of_AMD_FX_microprocessors). These isolated cases do not affect the general point that Intel dominates the high end of the MPU market.

[20] For models of pricing and innovation behavior in the MPU industry, see Aizcorbe and Kortum (2005), Nosko (2010), and Pillai (2013).

section investigates the properties of matched-model and hedonic indexes in the post-2006 pricing environment.

3. Constructing MPU Price Indexes

As noted, the changes in the pattern of Intel's posted MPU prices raise important questions for price measurement. Can a matched-model index correctly capture price trends given Intel's new pricing regime? If not, what approach to price measurement is likely to deliver estimates that are most robust to possible measurement error in prices? Finally, in an environment with rapid gains in MPU performance and changes in chip architecture, what are the best ways to measure quality change for MPUs?

In this section, we investigate these questions and make the case that — given the new pricing regime for MPUs that emerged in the mid-2000s — hedonic indexes are preferable to matched-model indexes. In addition, we argue that, given possible measurement error and current limitations on data availability, hedonic regressions that rely only on prices in the period of a model's introduction are likely to be more robust than hedonic regressions that include prices over a chip's entire life cycle. We also argue that hedonic indexes using actual measures of performance have important advantages over those using variables capturing physical characteristics of MPUs.

Matched-model or hedonic? To fix ideas, we briefly describe the matched-model and hedonic approaches to price measurement (see Aizcorbe, 2014, for a recent, in-depth treatment of this topic). Matched-model indexes control for quality change between two periods, say period 0 and period 1, by averaging price changes for models that were in the market in both periods. The underlying idea is to measure "pure" (or quality-adjusted) price change for products whose quality did not change because they were in the market in both periods 0 and 1.

Hedonic price indexes identify "pure" price change by explicitly controlling for quality change with measures of product characteristics or performance. The hedonic approach regresses prices on these measures, with the price change left after controlling for quality taken to be the quality-adjusted price change. Many alternative specifications have been proposed for hedonic regressions. Perhaps the simplest is to include time dummy variables (time fixed effects) in the hedonic regression and to read off quality-adjusted price change from the coefficients on the time dummies. (We discuss in section 5 our preferred specification for the new price indexes in this paper.)

To illustrate why we prefer hedonic over matched-model indexes for MPUs, we use stylized examples of Intel's pricing behavior to highlight the implications of the shift in behavior. Panel A of figure 8 illustrates the pricing pattern for Intel MPUs prior to the mid-2000s in which the price of each MPU model falls as it ages; this panel is a stylized version of the actual price cascade for 2000-01 shown previously. When a new, higher-quality model is introduced, the price of the old model falls so that price *per unit of quality* is at least roughly equalized across models. In this case, the gap between model prices in periods when two models are in the market would represent the value of improved quality, and a matched-model index would correctly adjust for this quality change.

Panel B shows a scenario in which prices of incumbent models do not fall when new, higher-quality models are introduced — a stylized version of the actual price cascade we presented for 2011-12. Given the upward trend in chip quality, price per unit of quality in panel B is falling as new models are introduced. However, a matched-model index would indicate that quality-adjusted prices are constant because the price of each model stays the same as it ages. Thus, a matched-model index would give a biased read of trends in quality-adjusted prices.

In contrast, a hedonic index that used appropriate measures of quality would correctly capture price trends even in the scenario in Panel B. In that scenario, prices are not changing, but the quality measure in the hedonic regression would account for the improvement in price-performance ratios when new models are introduced, and a hedonic index would show a downtrend in quality-adjusted prices reflecting the decline in price per unit of quality.

These scenarios illustrate why we believe that matched-model indexes will generate biased price trends in the period following the shift in Intel's pricing behavior, and why we believe that hedonic indexes are more likely to correctly capture price trends for MPUs.

Introduction-period or full-sample hedonic regressions? A natural starting point would be to assume that hedonic regressions should be estimated using all available data. However, under certain circumstances, a full-sample regression can lead to biased estimates of price change. For example, in the 1980s some researchers constructed price indexes for mainframe computers using only introduction-period prices for each model. This choice was made because of concerns that available IBM list prices for older models might not be actual transaction prices (see Cole et al., 1986).

We believe a similar concern may apply to MPUs. To explain why, we consider two possible explanations for what lies behind the pricing pattern adopted by Intel in the mid-2000s. Panel C of figure 8 shows a stylized scenario in which prices of older models are measured with error. Specifically, posted list prices in this scenario do not represent true transactions prices because Intel offers "age-related discounts" to selected purchasers as models age. In this scenario, new models enter the market at the same list price that exiting models leave the market, just as in panel B. We now add the dashed lines, which show actual transaction prices. These

lines slope downward, as progressively larger discounts are offered on older models as newer, higher performance models become available.

In the age-related discounting scenario, a full-sample hedonic index based on observable *posted* prices would go astray because the posted prices are measured with error. The actual transaction prices of each model are falling over time but a full-sample hedonic index would not account for this measurement error, leading to biased estimates of quality-adjusted price change.

In contrast, the introduction-period hedonic index could correctly capture trends in quality-adjusted prices if age-related discounts were offered as in panel C.[21] In particular, the introduction-period hedonic would omit observations in which prices were measured with error, and the performance variables in the regression would control for improvements in quality in successive periods.

Panel D highlights another scenario ("Drop-off in volume") that also could create challenges for a full-sample hedonic index. In this scenario, posted prices do not change, but in contrast to panel C, we assume they represent actual transaction prices. With this pricing assumption, the quantity purchased of a model drops off as it ages and faces competition from newer, more powerful models with lower prices per unit of quality. The solid, heavier line represents the early, high-quantity part of each model's life cycle and the thinner line represents the later part when sales have dropped. If model-level data on shipments or sales were available, a shipments- or sales-weighted index would account for the declining importance of the older model. However, model-level quantity data are not readily available. Accordingly, we (and other researchers) are forced to consider price indexes that put equal weight on every observation.

[21] The introduction-period index would capture price trends even if list prices at the time of introduction do not represent actual transactions prices provided that discounts at the time of introduction do not vary systematically over time or across models.

In the scenario illustrated in panel D, an unweighted full-sample hedonic index would put too much weight on price observations for which there were few transactions. In contrast, an unweighted introduction-period hedonic index likely would do a better job of capturing the trend in quality-adjusted prices. By focusing on prices at the beginning of each model's life-cycle, a regression that applies equal weights to all observations avoids over-weighting models whose quantities have dropped off.

For the reasons described here, we emphasize introduction-period hedonic indexes, although we also report full-sample indexes. Our preference does not reflect a belief that introduction-period indexes are inherently better, but rather the view that introduction-period indexes are likely to be more robust to the data limitations that hamper efforts to estimate recent trends in quality-adjusted MPU prices. In particular, we believe that an introduction-period hedonic will be more robust to measurement error in list prices (the age-related discount scenario) and to a lack of model-level shipments data that prevents the use of weighted regressions (the drop-off in volume scenario).

Performance measures or physical characteristics in hedonic regressions? A long-recognized challenge facing hedonic methods has been the choice of variables to include in the regression to control for quality. The typical approach has been to include measures of key physical characteristics of each model, in the belief that these characteristics will serve as a proxy for what purchasers value. This approach has raised concerns in the past, and researchers have called for the inclusion of actual performance measures rather than physical characteristics (see Triplett, 1989, and Berndt and Griliches, 1993). The underlying logic behind using performance measures is to focus on the output received by users rather than the input characteristics used to generate that output. For many products, measures of performance are

unavailable so there is little choice but to use characteristics. For MPUs, however, measures of performance — specifically for the types of tasks actually undertaken by users — are available as described above. Moreover, specifying an appropriate hedonic regression and finding suitable data can be difficult for a rapidly evolving product, and using directly measured performance helps to address this problem.

Accordingly, in this paper, we develop hedonic indexes with performance measures from SPEC that avoid the difficulties entailed in trying to capture quality for MPUs with rapidly changing architecture by identifying relevant physical characteristics. Our preferred performance metrics are described in detail in the next section.

4. Data

Prices and SPEC scores. Our MPU prices are collected from publicly available Intel price lists for the period from 1999 to 2013.[22] Intel announces wholesale list prices several times a year for MPUs sold in multiples of 1,000. Unlike single units sold in retail channels, these "trays" of MPUs do not include a cooling system and carry a shorter warranty. Models are identified by family (for example, Core i7, Pentium, Core 2 Duo), model ID (for example, i7-4960X), and selected technical characteristics (for example, amount of cache memory or clock speed). We merged these price lists to create price data at a quarterly frequency. We restrict our attention to the 373 MPU models for desktop computer systems introduced between 2000 and 2013.

To measure the relative quality of different chips we use the performance scores from SPEC that were mentioned in section 2. (These benchmark tests are described in detail in

[22] Price lists for the period from April 1999 to December 2006 were collected from an archived version of a website devoted to computer hardware. Price lists for later dates were obtained directly from Intel's website. On dates when both sources were available, we confirmed that the website prices matched Intel price lists.

appendix A.) Briefly, SPEC scores evaluate performance of an MPU on individual tasks that rely heavily on integer computation (such as word processing) and on tasks that rely heavily on floating point computation (such as speech recognition). Scores for individual tasks are measured in seconds, although SPEC rescales these scores so that higher scores indicate better performance and the units are no longer in seconds. SPEC provides an overall score both for integer and for floating-point computation, which are calculated as geometric means of scores for 12 integer computation tasks and 17 floating-point computation tasks, respectively. To construct a single measure of performance, we take the geometric mean of the overall scores for integer and floating-point tasks.[23]

SPEC scores are widely used to compare the performance of alternative MPUs or computers and also are used as a standard by computer engineers.[24] For example, Hennessy and Patterson (2012) — the standard text on computer design and architecture — notes that "One of the most successful attempts to create standardized benchmark application suites has been the SPEC (Standard Performance Evaluation Corporation) …" (p. 38). This textbook relies on SPEC scores to measure the growth in processor performance in recent decades.[25]

SPEC benchmarks provide several ways to measure MPU performance. The performance of a single task is measured by the "speed" score and the simultaneous performance of multiple tasks is measured by the "rate" score. The "speed" and "rate" scores differ in their use of parallel processing, an important consideration after the introduction of multi-core MPUs in the mid-2000s. In the "speed" test, a single task may be broken into component calculations to be run on different processing cores on the MPU. In the "rate" test, multiple instances of the

[23] Although the integer and floating-point scores could be included as separate variables in the hedonic regressions described below, little would be gained relative to the equal-weighted geometric mean, as the correlation between the two scores is greater than 0.98.
[24] One of our employers uses SPEC scores in making decisions about purchases of computing equipment.
[25] See figure 1.1 on page 3.

same task may be run simultaneously to more fully exploit the potential of the chip. We use the "speed" score as our base case, but the results using the "rate" score (available from the authors) are very similar.

Sample selection. We matched 184 MPU models from our price data, or 49 percent, to at least one performance score published by SPEC. An important question is whether this selection on the availability of SPEC scores could bias our results. Table 2 provides information on this point, showing a range of chip characteristics both for chips with SPEC scores and for those without scores.[26] As shown in Panel A of the table, average entry prices for chips with SPEC scores are considerably higher than for chips without SPEC scores. Perhaps not surprising given the difference in average prices, chips with SPEC scores tend to have technical features associated with higher performance. Clock speed is somewhat greater for chips with SPEC scores; the shift to multicore architecture occurred more quickly; and the amount of power used by the chip (thermal design power[27]) is greater. For the most part, these differences in technical features taken individually are not very large, and there is no consistent difference in the final characteristic shown in the panel — the size of the smallest feature on the chip (lithography).

For our purposes, the essential issue is whether price trends differ across the samples of chips with and without SPEC scores. To examine this question, we construct matched-model indexes using the PPI methodology (labeled PPI-like) for both samples. As shown in Panel B of the table, over the full period from 2000 to 2013, the average rate of decline in these PPI-like price indexes is very similar across the chips with and without SPEC scores (29 percent versus 26 percent, respectively). The two sets of chips also display similar price trends within the

[26] The information on characteristics is collected from Intel's product information database (http://ark.intel.com).
[27] Thermal design power (TDP) measures the amount of heat generated when running typical software for the chip. The amount of heat generated (measured in watts) is closely related to the MPU's power consumption.

shorter time periods shown in the table. The similarity of the price trends suggests that our results are not biased by the absence of SPEC scores for some chip models.

Representativeness of our sample relative to the PPI. A second important question is how well price trends in our sample track those in the PPI. Our sample is for Intel desktop chips, while the scope of the PPI includes desktop chips from other manufacturers (notably including AMD), as well as chips for servers and laptops. As can be seen in Panel B, our PPI-like indexes for Intel desktop chips and the PPI for all MPUs display very similar price trends. Accordingly, we are comfortable using our results for Intel desktop chips to draw inferences about the performance of the PPI.

5. Specification of the Hedonic Regressions

To fix ideas, we first describe a dummy-variable hedonic specification:

$$\ln(P_{i,t}) = \alpha + \sum_k \beta_k X_{k,i,t} + \sum_t \delta_t D_{i,t} + \varepsilon_{i,t} \qquad (1)$$

where $P_{i,t}$ is the price of chip i in period t, $X_{k,i,t}$ is the value of characteristic k for chip i in period t (measured in logs or levels, as appropriate), $D_{i,t \in Y}$ is a vector of time dummy variables (fixed effects) that equals 1 if chip i is observed in period t and zero otherwise, and $\varepsilon_{i,t}$ is an error term.

A potential shortcoming of equation 1, highlighted by Pakes (2003) and Erickson and Pakes (2011), is that the coefficients on the characteristic or performance variables are constrained to remain constant over the full sample period. One response to that concern is to run a cross-section regression for every time period and then to use results from those regressions to build up a price index.[28] Such an approach is appealing because it provides maximum flexibility for estimated coefficients to change over time and allows the results to be

[28] See Aizcorbe's (2014) discussion and the references there.

used in price index formulas. However, our sample size is too small to run reliable cross-section hedonic regressions for every quarter or even every year.

As a compromise, we focus on adjacent-period (in our case, adjacent-year) hedonic regressions.[29] Specifically, we estimate the following regression for each two-year overlapping period:

$$\ln(P_{i,t}) = \alpha + \sum_k \beta_k X_{k,i,t} + \delta D_2 + \varepsilon_{i,t} \qquad (2)$$

where $P_{i,t}$ is the price of chip i in year t. We measure $P_{i,t}$ as the average of the observed prices of chip i within the year.[30] The dummy variable D_2 equals 1 if the price observation is in the second year of the two-year overlapping period and 0 otherwise. To construct a price index from this sequence of regressions, we spliced together the percent changes implied by the estimated coefficients on the D_2 variables. In our main results, we rely on the SPEC variable to capture the performance of each MPU as experienced by users, so that $\sum_k \beta_k X_{k,i,t}$ reduces to $\beta \ln(SPEC_{i,t})$.

As noted in the previous section, SPEC updated its suite of performance tests in 2006. We use the older (SPEC 2000) benchmarks for the adjacent-year regressions through 2005-06 and the newer (SPEC 2006) benchmarks for the adjacent-year regressions beginning with 2006-07.

As a comparison, we also estimate equation 2 with a set of chip characteristics on the right-hand side instead of the SPEC variable. This alternative regression represents the usual approach to hedonic specification in the literature and allows us to gauge the effect on estimated price trends of controlling directly for performance. The characteristics included in the regression are those shown in table 2 — clock speed (in gigahertz), number of cores, maximum

[29] See Triplett (2006) for a discussion of adjacent-period hedonic regressions.
[30] We also estimated regressions at the quarterly frequency for each two-year period and included a time trend spanning the eight quarters of data included in each regression. That alternative yielded price trends similar to those reported here.

thermal design power (in watts), and lithography size (in nanometers) — plus cache memory (in megabytes), a dummy for whether the chip has a separate graphics processing unit, and the number of threads.[31] We use the natural log of clock speed, thermal design power, lithography size, and cache memory; the number of cores and number of threads enter the regression in levels.

6. Results

Table 3 shows estimates of equation 2 using SPEC performance for the overlapping two-year periods during 2000-06, and table 4 shows estimates for 2006-13. The upper panel in each table presents estimates that rely only on prices in each MPU model's introduction period, while the lower panel presents estimates based on the full sample of price observations. The coefficient on the second-year dummy variable in each adjacent-year regression measures the rate of change in quality-adjusted MPU prices from the first year to the second.

Overall, the regressions explain much of the variation in MPU prices. The adjusted R^2 averages close to 0.50 across the full set of regressions shown in tables 3 and 4.

Although Pakes (2003) cautions against providing structural interpretations of the coefficients, we note that the coefficients on SPEC performance are uniformly positive and significant at the 5 percent level. These coefficients indicate that higher performing MPU models sell for higher prices and suggest that the performance measure captures an important element of the quality differences across MPU models.

Analogous tables for the regressions that replace SPEC performance with chip characteristics are provided in appendix C. These regressions fit the data well, with an average adjusted R^2 of about 0.75. Some of the estimated coefficients are in line with expectations. In

[31] MPUs can perform multiple threads—sequences of related program instructions—either by employing multiple cores or by sharing resources on an individual core. Thus, additional threads provide a form of parallel processing.

particular, the coefficients on clock speed, number of threads, and cache memory are generally positive and significant, with no instances of significant negative coefficients. In contrast, the significant coefficients on thermal design power, number of cores, lithography, and the graphics processor dummy change sign at least once. In addition, the significant coefficients on the graphics processor dummy are generally negative. Overall, these regressions exhibit the interpretational issues that often attend hedonic regressions estimated with a vector of product characteristics.[32]

To construct annual price indexes from the SPEC and characteristics regressions, we set the 2000 value of the index to 100, and then move the index forward year by year with the implied percent change from each adjacent-year regression. For example, to calculate the percent change from 2000 to 2001, we exponentiate the coefficient on the year dummy in the 2000-01 regression.[33] We then do the same for the 2001-02 regression, and so on.

We summarize our results in table 5 and figure 9. The table reports average rates of price change over 2000-04, 2004-08, and 2008-13 from six different measures: the hedonic index based on SPEC performance and introduction-period prices (our preferred index), three other hedonic indexes including those using chip characteristics, the MPU price index constructed by

[32] For completeness, we also estimated a version of the hedonic regression that included both SPEC performance and chip characteristics as controls for quality. The results were not crisp, as might be expected given the inclusion of both a summary measure of performance and chip features that influence the summary measure. In particular, the coefficient on SPEC performance was positive and significant in less than half of the regressions and insignificant in the rest. The coefficients on the characteristics, though broadly similar to the characteristics-only regression, displayed more frequent instances of significant changes in sign.

[33] Because the exponential function is nonlinear, the translation from the natural log of prices to price levels requires an adjustment in order to be unbiased. We apply the standard adjustment based on the estimated variance of the regression error; see Aizcorbe (2014) for details. This adjustment had very little effect on estimated price trends over 2000-04, but over 2004-08 and 2008-13 it slowed the estimated annual rate of price decline by as much as 10 percentage points relative to the unadjusted estimates.

the Federal Reserve Board, and the PPI.[34] The figure plots the levels of the PPI and the two hedonic indexes based on SPEC performance.

From 2000 to 2004, all of the indexes show very rapid declines in MPU prices. As discussed in section 3, with Intel's ubiquitous downward re-pricing of existing chips before the mid-2000s, all of the price indexes—both matched model and hedonic—would be expected to capture the downward trend in quality-adjusted prices. This expectation is borne out by our results. As shown in table 5, all of the MPU price indexes fell at an average annual rate of 39 percent or more over 2000-04. In addition, the rate of decline in the PPI (and the Fed's index) is very similar to that of our preferred hedonic index.

However, the trends in the indexes diverge after 2004. Although our preferred hedonic index fell somewhat less rapidly after 2004 than before, the decline in the PPI slowed much more sharply. Indeed, the PPI fell at an average annual rate of only 8 percent from 2008 to 2013 and barely declined at all in 2012 and 2013. For the reasons highlighted earlier in the paper, we believe that this divergence points to likely bias in the PPI for MPUs and suggests that the PPI could be providing a deeply misleading picture of price trends for MPUs in recent years.[35]

The full-sample hedonic index based on SPEC performance declined less rapidly than the introduction-period index in each period, with the largest difference occurring after 2008. As indicated by the analysis in section 3, the wider gap after the mid-2000s is what would be expected under the "age-related discounting" and "drop-off in volume" scenarios if Intel were keeping posted prices for older models fixed to a greater degree than previously. Because

[34] The Federal Reserve series is a matched-model index from 1992 to 2006 linked to an introduction-period hedonic index after 2006. The hedonic index is constructed from an earlier version of the empirical work presented here.
[35] In a closely related study, Sun (2014) estimated hedonic regressions for MPUs used in laptops. Because SPEC scores were not available for a wide enough set of laptop chips, Sun used a variety of other performance benchmarks in the regressions. She found that prices for laptop MPUs trended down at a 20 to 30 percent average annual pace over past ten years, depending on the regression specification. The rate of price decline slowed after 2010, though not to the extent shown by the PPI.

discounts from posted prices are unobservable, the full-sample index will understate price declines to the extent that Intel is discounting older models; this bias will be larger than when posted prices were more flexible. Moreover, to the extent that Intel is allowing price-performance ratios on older models to rise above those for new models, sales of the older models likely are falling off more substantially than when posted prices fell over a chip's life cycle. Given that we do not have model-level shipments data, the index based on the unweighted full-sample index would overweight the older models whose prices are not changing. Under either scenario (or a combination of them), the full-sample hedonic index will understate the rate of price decline, supporting our preference for the introduction-period index.[36]

The post-2004 slowing in estimated price declines is much more pronounced in the regressions that use chip characteristics than in those using SPEC performance. As shown in table 5, during 2004-08 and 2008-13, the price indexes obtained from the characteristics-based regressions fell at average annual rates ranging from only 1 percent to 21 percent, a far slower rate of decline than in the corresponding SPEC-based indexes.

The wide gap stems from the post-2004 divergence between the continued performance gains indicated by SPEC scores and the flat path for chip quality implied by the characteristics regression (which we demonstrate below). With no quality improvement, the characteristics regression "thinks" that constant-quality prices are no longer falling more rapidly than observed list prices.

[36]As a robustness check for the introduction-period SPEC regression, we estimated an alternative version that included not only chip prices in the quarter of introduction but also prices in the three quarters following the chip's introduction. The price index obtained from this regression fell at a (bias-adjusted) annual rate of 38 percent, 34 percent, and 39 percent, respectively, over 2000-04, 2004-08, and 2008-13. Thus, MPU price declines are estimated to have remained rapid whether we use only the introduction-period price or broaden the sample to include prices observed within a year of introduction.

To measure the implied change in chip quality over time, recall from equation 2 that the effect of quality on the log of observed chip price in the adjacent-year regression is $\sum_k \beta_k X_{k,i,t}$. Letting t_1 and t_2 denote the first and second of the two adjacent years, the average value of the quality effect for the chips that appear in the regression in t_1 is $\sum_k \beta_k \bar{X}_{k,t_1}$, with an analogous expression for t_2. Thus, the change in the quality effect from t_1 to t_2 is $\sum_k \beta_k \left(\bar{X}_{k,t_2} - \bar{X}_{k,t_1}\right)$.[37] When SPEC performance is used as the sole control for chip quality, this expression reduces to $\beta\left(\bar{X}_{t_2} - \bar{X}_{t_1}\right)$, where *X* is ln(*SPEC*). It is important to note that $\sum_k \beta_k \left(\bar{X}_{k,t_2} - \bar{X}_{k,t_1}\right)$ measures the effect of quality change on prices, not the pure change in quality itself. However, on the reasonable assumption that higher quality is associated on average with higher chip prices, the sign of $\sum_k \beta_k \left(\bar{X}_{k,t_2} - \bar{X}_{k,t_1}\right)$ indicates whether chip quality is improving, worsening, or remaining unchanged, which is sufficient for our purpose.

Figure 10 shows the time series for the price effect of chip quality, measured from each adjacent-year regression as $\sum_k \beta_k \left(\bar{X}_{k,t_2} - \bar{X}_{k,t_1}\right)$, with each year-pair then linked together to form the time series. The β coefficients and the average chip characteristics are both taken from the introduction-period version of the regressions, and thus represent the price effect of quality at the frontier. As can be seen, the SPEC-based series rises every year, implying a sustained increase in chip quality; this result is consistent with the direct measure of SPEC performance that was shown previously in figure 1. In contrast, the series based on chip characteristics in figure 10 only edges up on net after 2003, implying little effect on prices of the improvement in chip quality from that year forward, punctuated by a sizable decline in 2008. Interestingly, the characteristics-based series in figure 10 bears a striking resemblance to the series for clock speed

[37] Aizcorbe (2006) also measures the price effect of changes in chip quality. Although her method involves taking the difference between the changes in observed prices and quality-adjusted prices, algebraically this is very close to what we do.

in figure 1. Thus, even though the characteristics-based regression includes seven MPU characteristics, clock speed exerts a powerful influence on the implied measure of chip quality in the regression.

These results raise questions about the constant-quality MPU price indexes obtained from the regressions that control for quality with chip characteristics. To view those indexes as credible, one must accept either that the quality of MPU chips was essentially stagnant for the decade after 2003 or that the market placed no value on rising performance over that decade. The second condition is implausible on its face, while the first implies that the upward march in chip quality indicated by SPEC ratings — the industry standard for performance measurement — is spectacularly wrong. The much more likely conclusion, in our view, is that chip performance has continued to improve and that constant-quality MPU prices have remained on a steep downtrend.

7. Conclusion

After falling rapidly through the mid-2000s, the PPI for MPUs has declined very slowly by historical standards in recent years. Such a slowdown is puzzling given evidence of ongoing rapid advances in semiconductor technology. To reconcile these observations, this paper demonstrates that the matched-model procedure used for the PPI for MPUs likely is inappropriate in the pricing regime that Intel — the dominant manufacturer — adopted in the mid-2000s. We argue that a hedonic approach based on introduction-period prices is the preferred way to measure quality-adjusted MPU prices in the current pricing environment. We implement this hedonic approach with an MPU performance measure that addresses

longstanding concerns in the literature about the use of product characteristics to proxy for performance.

The results from our preferred hedonic price index indicate that quality-adjusted MPU prices continued to fall rapidly after the mid-2000s, contrary to the picture from the PPI. Our results have important implications for understanding the rate of technical progress in the semiconductor sector and, arguably, for the broader debate about the pace of innovation and its implications in the U.S. economy. Notably, concerns that the semiconductor sector has begun to fade as an engine of growth appear to be unwarranted. Rather, these results suggest continued rapid advances in technologies enabled by semiconductors.

That said, it is important to highlight that our results have limited direct implications for the measurement of real GDP or output per hour. Semiconductors mostly are intermediate inputs and so are not counted directly in GDP. Imports and exports are the exception, but trade quantities are small enough that, even if our preferred price indexes for MPUs were adopted, measures of real GDP growth would change by only a small amount.

As a final point, we note that our results raise a new puzzle. In recent years, the price index for computing equipment in the National Income and Product Accounts has fallen quite slowly by historical standards. If MPU prices have, in fact, continued to decline rapidly, why have prices for computers — which rely on MPUs for their performance — not followed suit? We believe there is a reasonable chance that the official price indexes for computers have been measured with error, reflecting in part the challenge of identifying the relevant and likely changing set of physical characteristics used to measure quality. The end-user performance measure employed in this paper could help break this knot for computer prices, and we are investigating this possibility in further work.

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Table 1. Semiconductor Technology Cycles
(Years needed for 30 percent reduction in linear scaling)

Industry Frontier			Intel MPU Chips	
Period	Years		Period	Years
1969-1993	3.0		1971-1994	2.9
1993-2012	2.1		1994-2012	1.9
1993-2003	1.9		1994-2004	1.9
2003-2012	2.3		2004-2012	2.0

Source. Byrne, Oliner, and Sichel (2013).

Table 2. Sample Characteristics: Is Sample Selection a Problem?

Panel A: Number of Intel models, characteristics, and price levels, by year of introduction

	2000-04	2005-08	2009-13
Number of Intel desktop MPU models			
With SPEC available	38	60	86
No SPEC available	47	45	97
Universe	85	105	183
Entry price ($)			
With SPEC available	512	416	243
No SPEC available	181	197	168
Clock speed (ghz)			
With SPEC available	2.07	2.86	3.00
No SPEC available	1.95	2.80	2.76
Number of cores			
With SPEC available	1.0	2.25	3.09
No SPEC available	1.0	1.44	2.76
Maximum thermal design power (watts)			
With SPEC available	60.3	92.3	75.1
No SPEC available	55.2	78.8	59.1
Lithography size (nanometers)			
With SPEC available	147.9	65.2	31.3
No SPEC available	134.7	73.9	30.9

Panel B: Price changes (percent, average annual rate)

	2000-04	2004-08	2008-13	2000-13
PPI-like matched-model price index (Intel MPUs)				
With SPEC available	-56	-19	-7	-29
No SPEC available	-48	-24	-6	-26
All desktops	-53	-22	-6	-28
PPI	-48	-29	-8	-28

Source. Authors' calculations based on data from System Performance Evaluation Corporation, Intel price lists, and data from http://ark.intel.com.

Table 3. Regression Results for 2000-06

Panel A: Introduction period only

	2000-01	**2001-02**	**2002-03**	**2003-04**	**2004-05**	**2005-06**
Year dummy	-.895** (.177)	-.363 (.209)	-.995** (.287)	-.929* (.281)	-.263 (.277)	-.819* (.311)
ln *Performance*	.63* (.27)	1.12** (.29)	2.98** (.69)	3.99** (.80)	4.39** (1.01)	2.95** (.74)
Number of Obs.	20	18	14	11	23	28
Adjusted R^2	.56	.48	.56	.70	.44	.34

Panel B: Full sample

	2000-01	**2001-02**	**2002-03**	**2003-04**	**2004-05**	**2005-06**
Year dummy	-.875** (.097)	-.318** (.072)	-.403** (.090)	-.489** (.115)	-.436** (.124)	-.494** (.092)
ln *Performance*	1.05** (.15)	.87** (.09)	1.13** (.12)	2.81** (.26)	3.15** (.35)	2.52** (.28)
Number of Obs.	100	111	94	78	107	157
Adjusted R^2	.46	.44	.47	.62	.43	.35

Note: The dependent variable is ln(MPU price); the regression includes a constant, not shown above. Standard errors are in parentheses. * and ** indicate significance at the 5% and 1% levels, respectively.

Table 4. Regression Results for 2006-13

Panel A: Introduction period only

	2006-07	2007-08	2008-09	2009-10	2010-11	2011-12	2012-13
Year dummy	-.726 (.388)	-.784* (.226)	-.754 (.369)	-.335 (.244)	-1.229** (.226)	-.481** (.110)	-.533** (.091)
ln *Performance*	1.87* (.76)	2.39** (.82)	2.86** (.70)	2.79** (.65)	3.31** (.50)	2.88** (.31)	2.88** (.20)
Observations	24	26	27	25	35	50	31
Adjusted R^2	.16	.28	.41	.41	.58	.65	.87

Panel B: Full sample

	2006-07	2007-08	2008-09	2009-10	2010-11	2011-12	2012-13
Year dummy	-.743** (.140)	-.533** (.112)	-.555** (.082)	-.177** (.064)	-.436** (.069)	-.469** (.068)	-.203** (.054)
ln *Performance*	2.22** (.28)	2.19** (.22)	1.73** (.14)	1.53** (.09)	1.14** (.09)	1.21** (.11)	2.98** (.16)
Observations	88	141	187	217	281	294	214
Adjusted R^2	.41	.41	.46	.57	.35	.29	.63

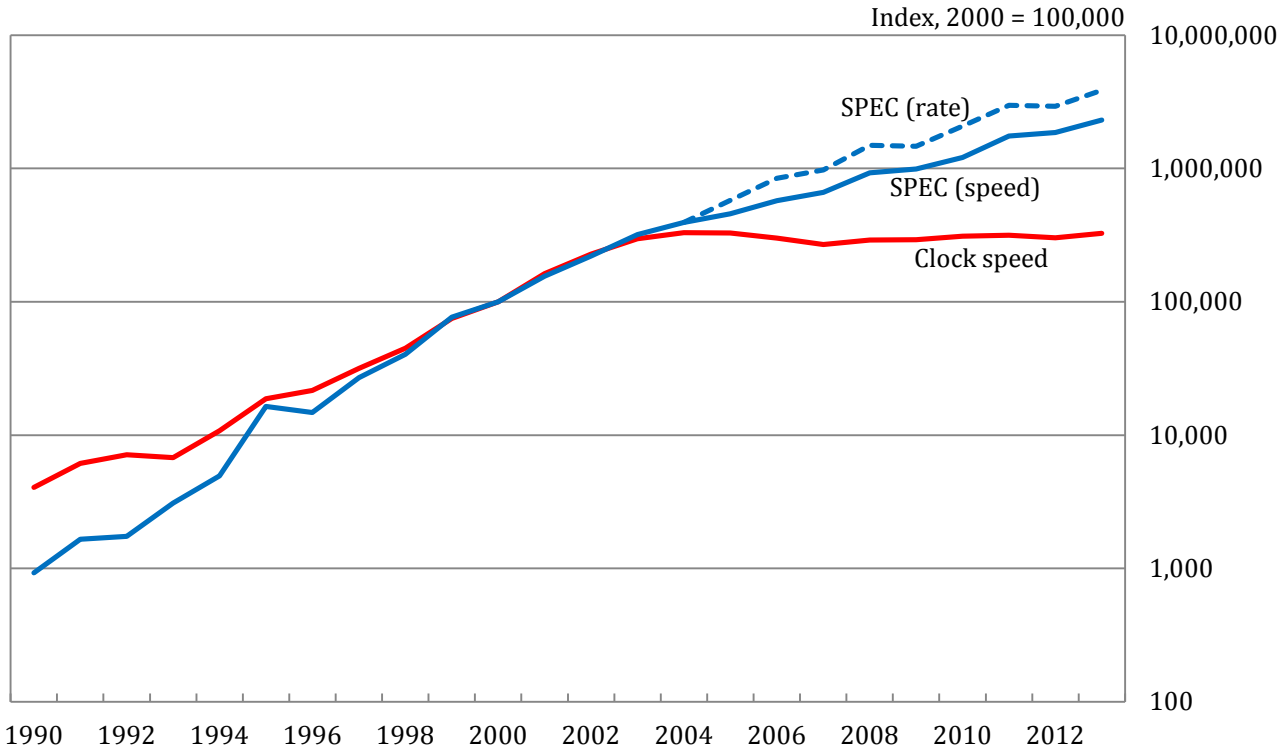
Note: The dependent variable is ln(MPU price); the regression includes a constant, not shown above. Standard errors are in parentheses. * and ** indicate significance at the 5% and 1% levels, respectively.

Table 5. Rates of change in MPU prices[1]
(Average annual percent change over periods shown)

	2000-04	2004-08	2008-13	2000-13
Hedonic, SPEC performance				
Introduction period	**-52**	**-37**	**-43**	**-44**
Full sample	-40	-33	-22	-31
Hedonic, chip characteristics				
Introduction period	-43	-1	-21	-23
Full sample	-39	-16	-13	-23
Federal Reserve Board[2]	-51	-29	-31	-38
PPI	-48	-29	-8	-28

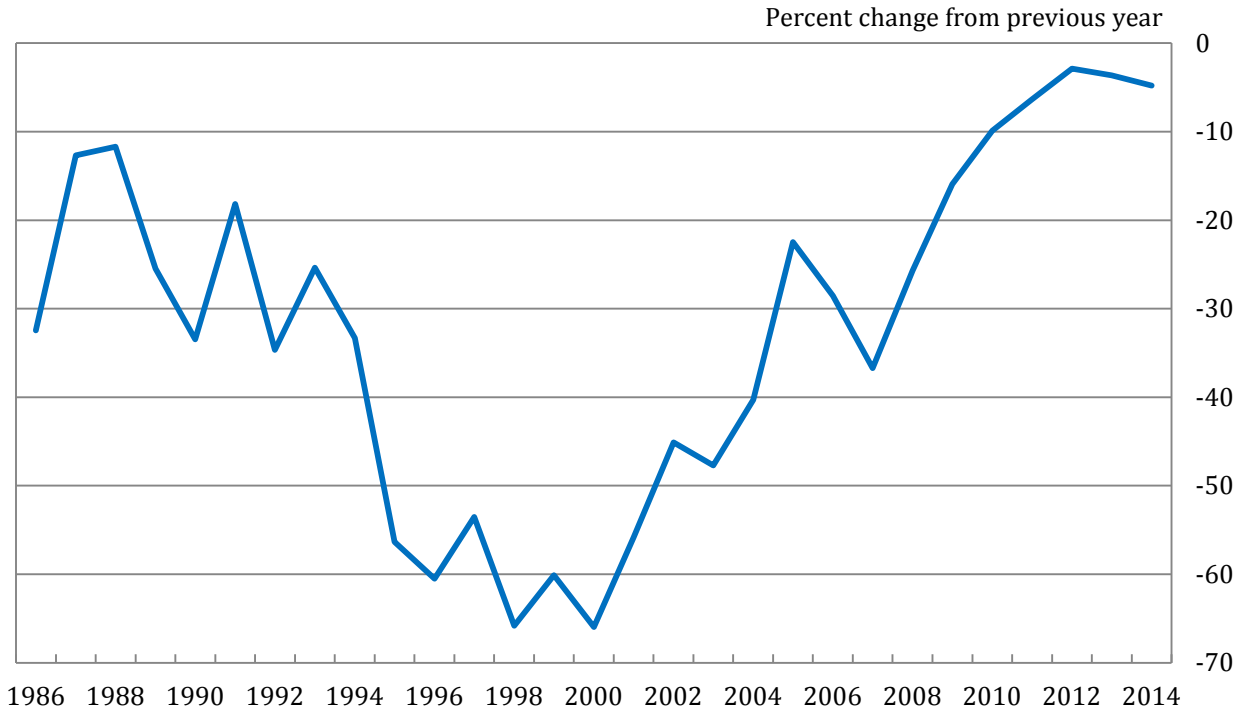
1. The results for the hedonic regressions have been bias-corrected for the conversion from the natural log of price to the price level. See the text for details.
2. Constructed as a matched-model index through 2006 and as an introduction-period hedonic index after 2006. The dataset and hedonic regression specification reflect an earlier version of the empirical work presented in this paper.
Source. Authors' calculations and Bureau of Labor Statistics.

Figure 1: Desktop MPU Performance Measures



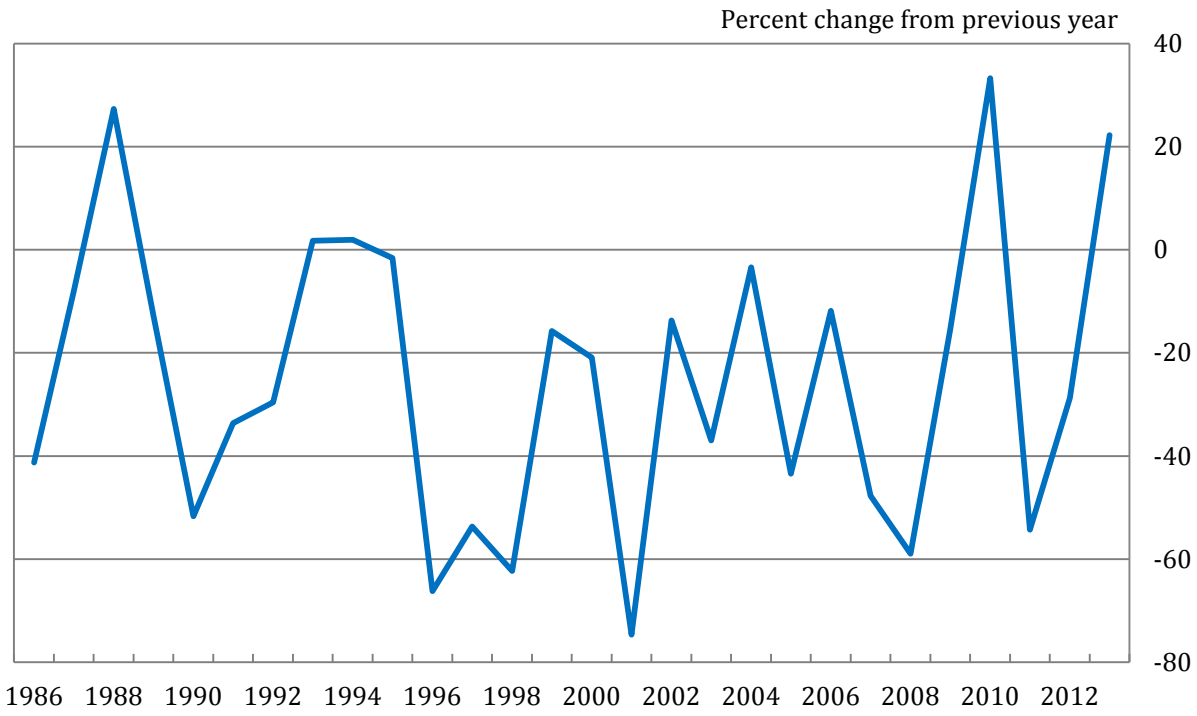
Source. Authors' calculations using data provided by Unni Pillai and performance information from Intel price lists and SPEC corporation.

Figure 2: Reported MPU Prices



Sources. Grimm (1998, table 12) for 1986-92, Federal Reserve Board for 1993-97, and Bureau of Labor Statistics for 1998-2014.

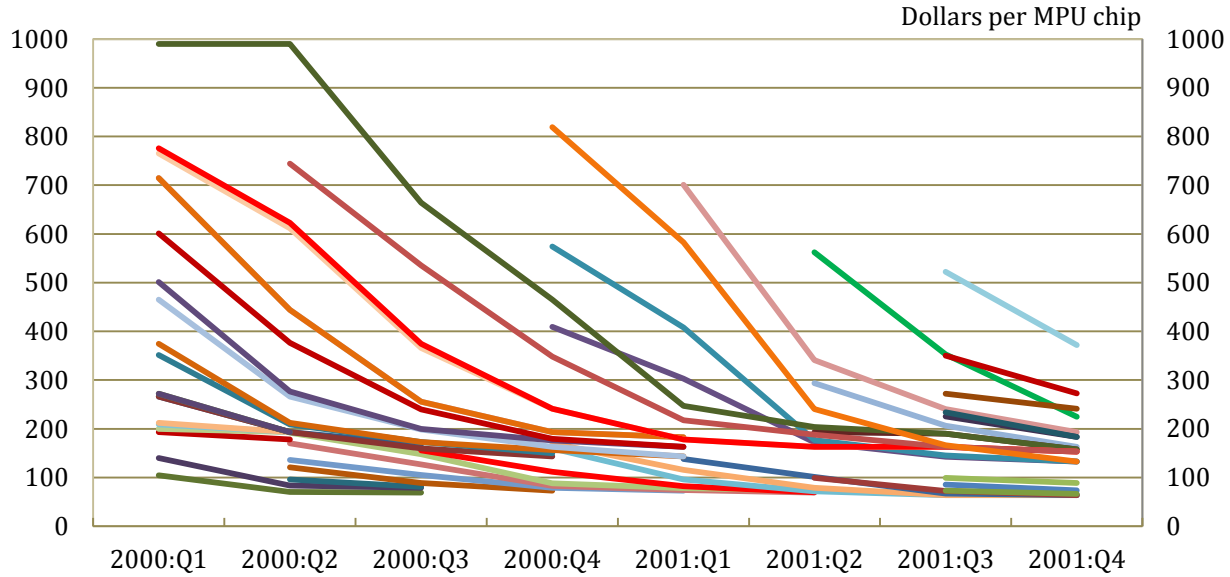
Figure 3: DRAM Prices



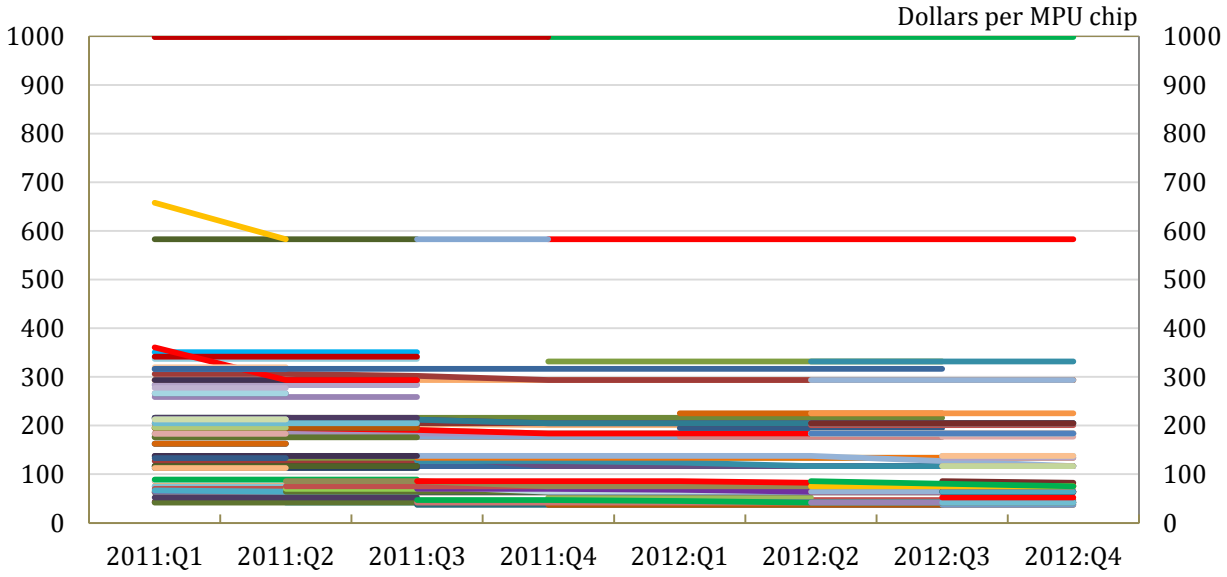
Sources. Grimm (1988, table 5) for 1986-92 and Federal Reserve Board for 1993-2013.

Figure 4: Intel List Prices

Panel A: 2000-01

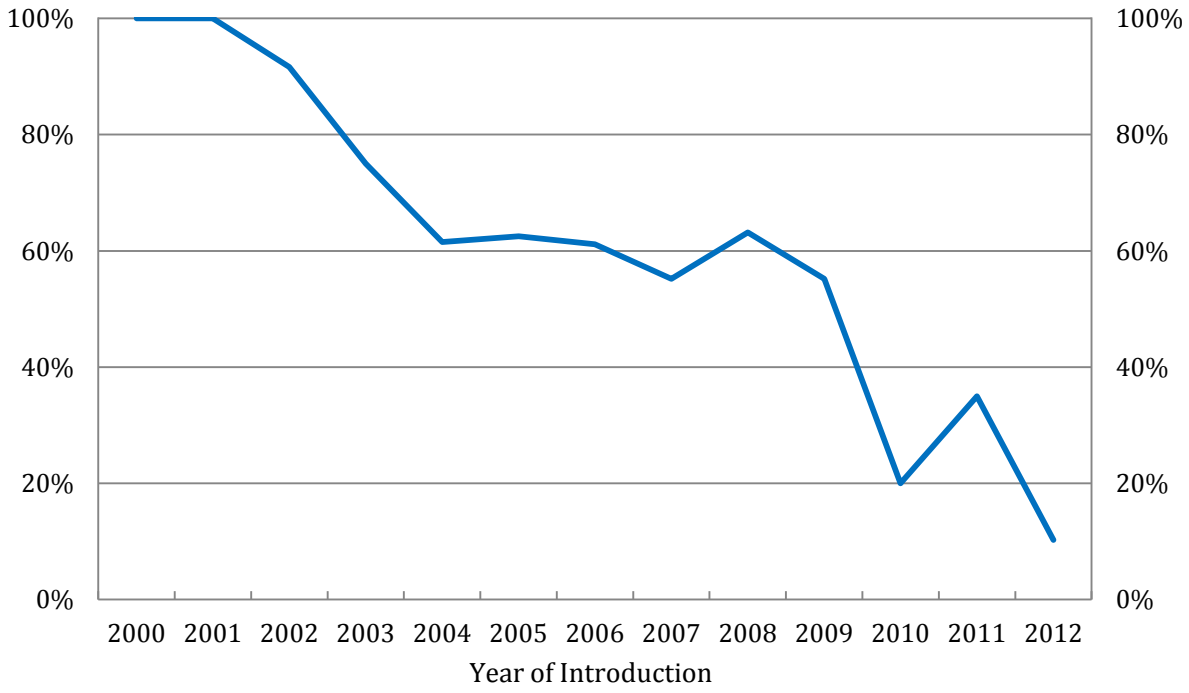


Panel B: 2011-12



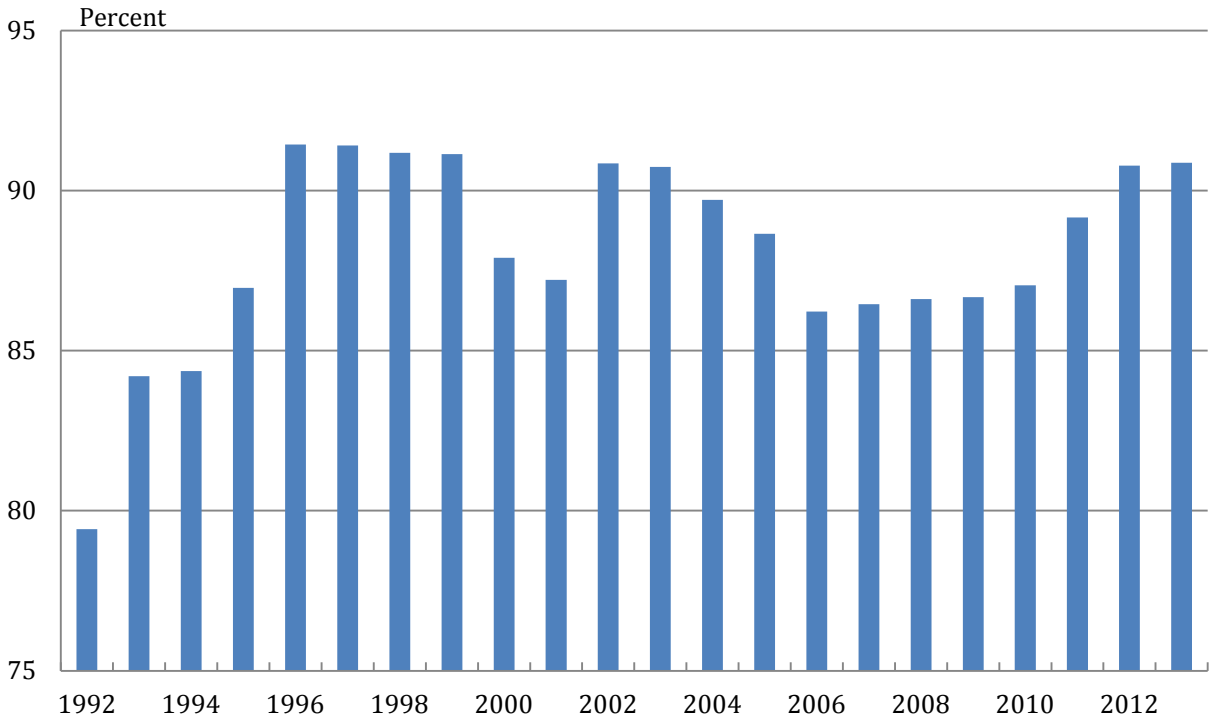
Note. Prices for 1,000 unit "trays" of MPUs.
Source. Authors' calculations from Intel price lists.

Figure 5: Share of Intel Desktop MPUs with List Price Decline within Four Quarters of Introduction



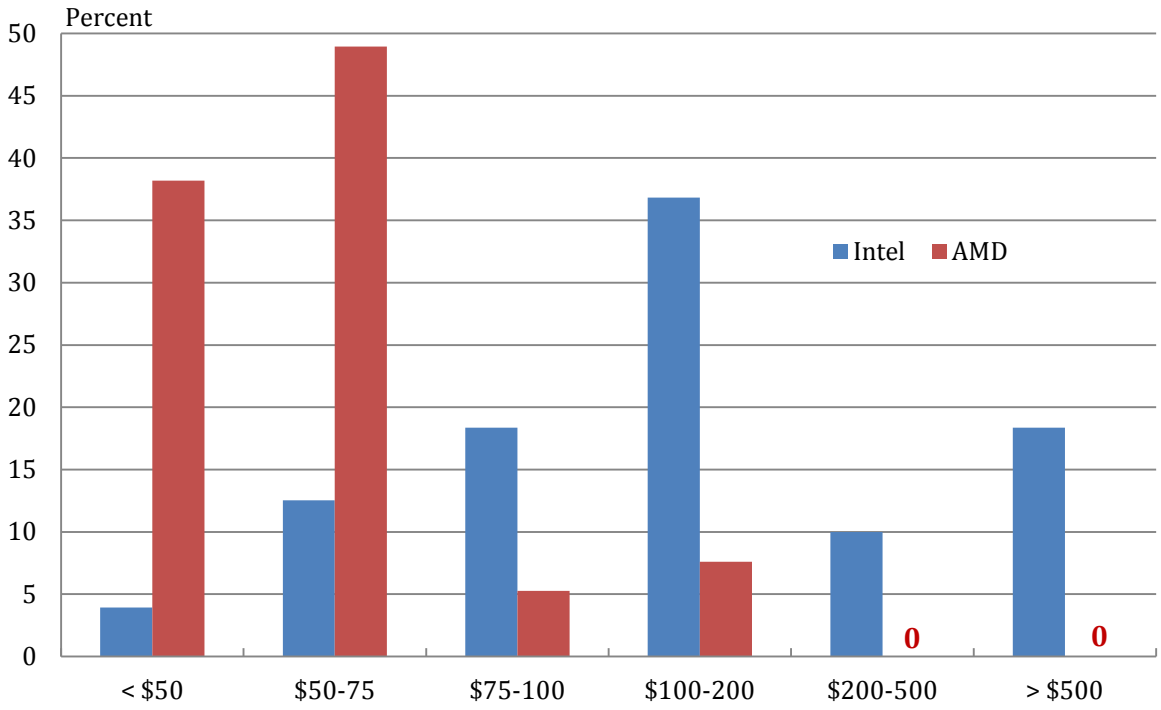
Source. Authors' calculations from Intel price lists.

Figure 6: Intel Share of Combined Intel and AMD Revenue



Source. Authors' calculations based on data from financial reports filed with the Securities and Exchange Commission.

Figure 7: 2013 Distribution of Desktop MPU Revenue, by Price of Chip



Note. Data cover 2013:Q1 through 2013:Q3.
Source. Authors' calculations based on data from IDC Research, Inc.

Figure 8: Alternative Scenarios

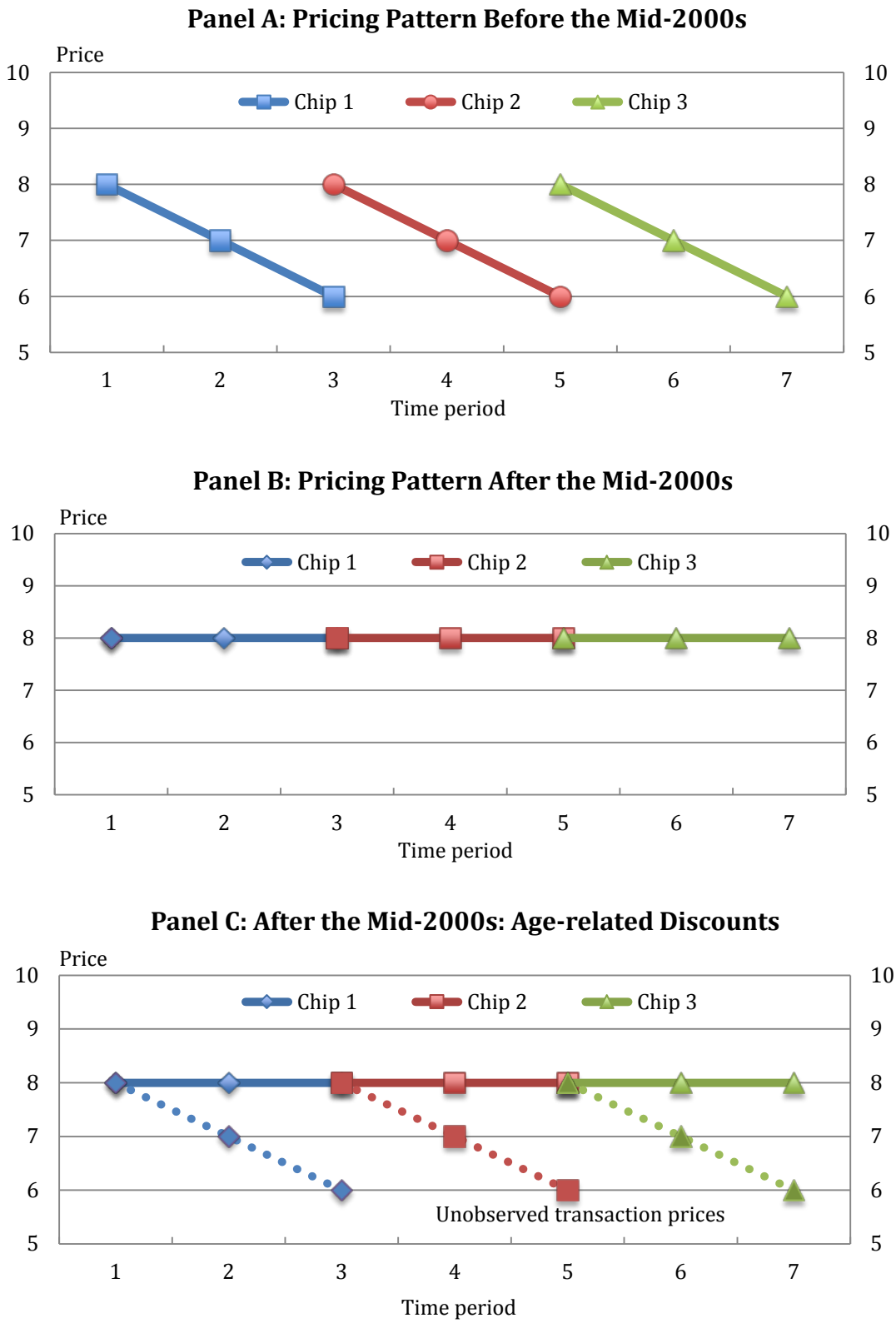


Figure 8: Alternative Scenarios

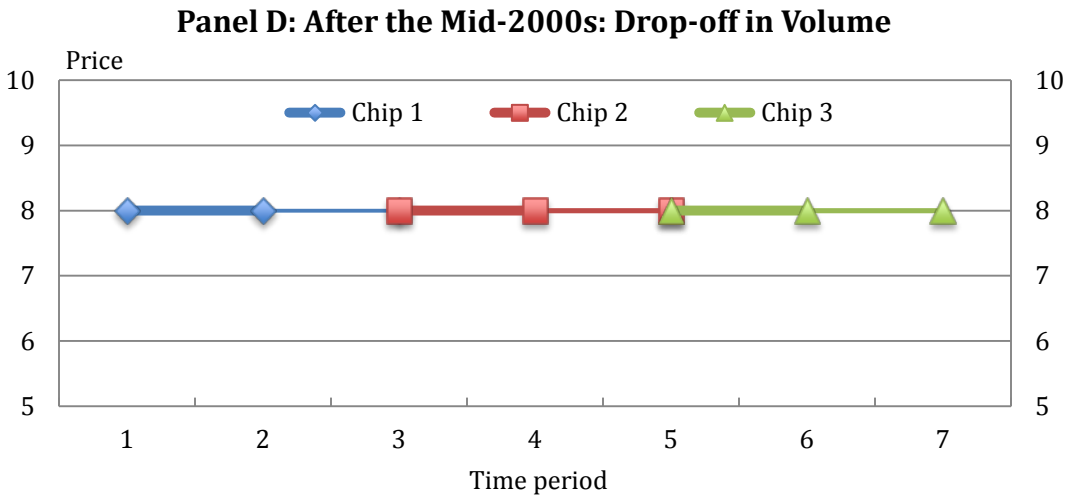
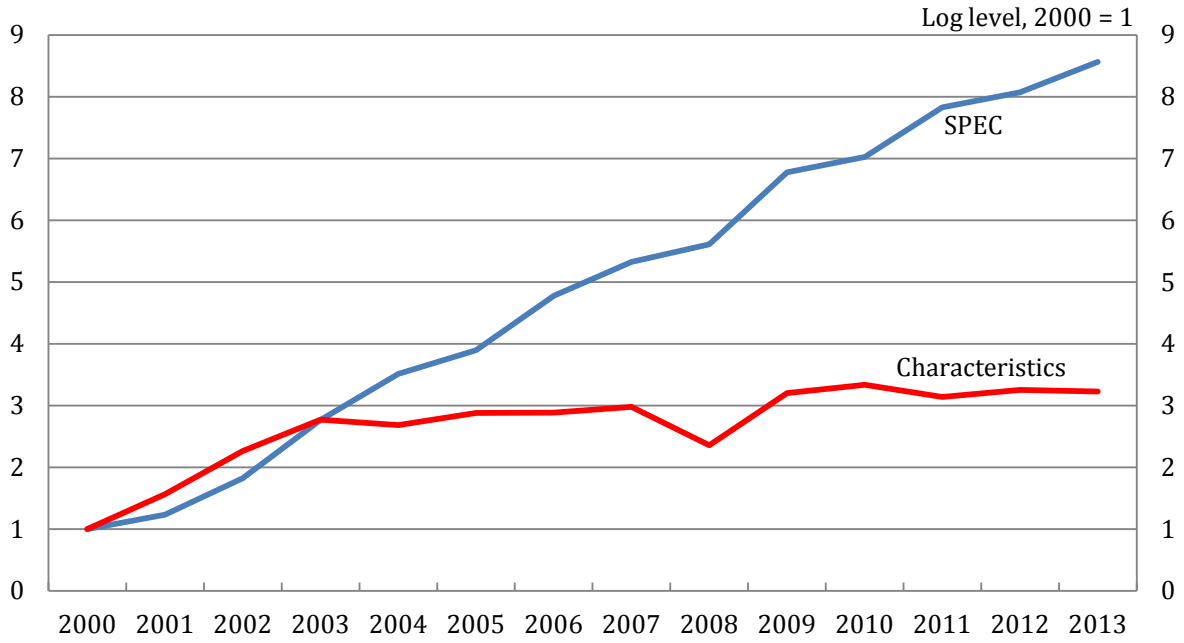


Figure 9: MPU Price Levels

Note. Hedonic indexes are based on regressions that use SPEC performance to control for quality.
Source. Bureau of Labor Statistics and authors' calculations.

Figure 10: Effect of Chip Quality on Price



Source. Authors' calculations. See text for details.

Appendix A: Performance Measures from SPEC (System Performance Evaluation Corporation)

As noted in the text, SPEC is a non-profit corporation that develops performance benchmarks for computers. This appendix describes the performance benchmarks from SPEC that we use in our analysis.

For MPUs, SPEC has developed a suite of benchmark tests that evaluate how quickly an MPU can complete a set of tasks that are developed from real user applications. These benchmark suites are updated periodically to reflect changes in MPU architecture and in relevant tasks. We use the latest benchmark, called CPU2006, as well as CPU2000.

The performance of an MPU will depend on characteristics of the system other than just the MPU; these other elements include memory and the compiler used. SPEC has benchmarks for a standard configuration ("base" metrics) and a configuration in which compilers are tuned for maximum performance ("peak" metrics). We use the base metrics.

Further details are provided below on how we use the CPU2006 and CPU2000 benchmarks to construct the performance measure used in our analysis.

CPU2006

CPU2006 was introduced in 2006, and we use results from CPU2006 to measure the performance of chips from 2006 to 2013. This benchmark consists of two suites of tasks. The first suite contains 12 tests that focus on integer calculations, and the second suite contains 17 tests that focus on floating point calculations. For each test, SPEC normalizes the test time by taking the ratio of the test time on a standardized reference machine to the test time for the MPU being tested. By scaling results in this way, shorter test times result in higher performance scores. SPEC then constructs a composite score for calculations by taking the geometric mean of the normalized individual integer scores; SPEC constructs a composite floating-point score in a parallel manner. The composite scores we use are called SPECint_base2006 and SPECfp_base2006.

As noted, these tests cover actual user applications. The integer and floating-point applications include the following.

- ***Integer*** applications include running PERL scripts, file compression, running a C compiler, combinatorial optimization, artificial intelligence (playing the games Go and chess), searching gene sequences, simulating a quantum computer, video compression, discrete event simulation, running path-finding algorithms, and XML processing.

- ***Floating-point*** applications include computations for fluid dynamics, quantum chemistry, quantum chromodynamics, molecular dynamics, general relativity, finite element analysis, linear programming, image rendering, structural mechanics, computational electromagnetics, weather modeling, and speech recognition.

To construct the performance measure used for most of our analysis, we take the geometric mean of the integer and floating-point composites described above.

With the advent of parallel processing, SPEC began distinguishing between *speed* and *rate* measures of performance. Speed measures focus on how fast a computer completes a single task. Rate measures focus on how many tasks a computer can complete in a given amount of time, taking advantage of available parallel processing.[38] The integer and floating-point performance suites described above are speed measures. Our analysis primarily focuses on these speed measures as they are available over a longer time span. That said, we also consider rate measures to more fully account for parallel processing and the rise of multicore chips.

CPU2000

CPU2000 was introduced in 1999 and retired in 2007. We use results from CPU2000 to measure the performance of chips from 2000 to 2006. The calculation of CPU2000 is very similar to that of CPU2006 except that the individual performance tests are of a type appropriate to the computing environment in the earlier period. The CPU2000 integer suite includes 12 tests, and the floating-point suite includes 14 tests.

Just as with CPU2006, for CPU2000, our analysis relies on the geometric mean of the integer and floating-point composite metrics, which themselves are geometric means of normalized results of the individual integer and floating-point tests.

Additional Details

We are able to bridge across the SPEC2000 and SPEC2006 benchmarks because results for 2006 were reported on both benchmarks for many chips. This allows us to estimate hedonic regressions for adjacent pairs of years through 2005-06 using SPEC2000 and for adjacent pairs of years starting with 2006-07 using SPEC2006.

An MPU chip often has multiple scores for each of the SPEC benchmark tests. Multiple scores can arise either because more than one computer vendor tested the chip or because a given vendor tested the chip under different conditions. The variation in test conditions can reflect differences in hardware (e.g., the circuit board or amount and type of DRAM) or software (e.g., the operating system or compiler). When multiple scores are available for a specific model, we use the model's median score.

[38] Speed scores do account for some parallel processing; in particular, speed scores allow for auto-parallelization for a single task, and by 2014 almost all speed scores reported using this feature.

Appendix B: Intel Desktop MPUs on Wholesale Price Lists

The table below (see next page) lists every Intel desktop MPU shown on the company's wholesale price lists starting in 1999. The most recent price list is posted at http://www.intc.com/pricelist.cfm; price lists for earlier periods were collected from this location and other online sites. Entry year denotes the year that the MPU first appeared on a price list. The MPU description is taken directly from Intel's ARK database, located at http://ark.intel.com, which contains a full history of Intel microprocessors; the note at the bottom of the table describes the minor ways we edited the ARK description to save space. The final column shows whether a SPEC score exists for each model. All of the models with a SPEC score are included in our empirical analysis. Of 373 models introduced by Intel during the period, 184 have SPEC scores available.

Entry Year	MPU Description[1]	SPEC Score?
1999	Celeron® 333 MHz, 128K Cache, 66 MHz FSB	No
1999	Celeron® 366 MHz, 128K Cache, 66 MHz FSB	No
1999	Celeron® 400 MHz, 128K Cache, 66 MHz FSB	No
1999	Celeron® 433 MHz, 128K Cache, 66 MHz FSB	No
1999	Celeron® 466 MHz, 128K Cache, 66 MHz FSB	No
1999	Celeron® 500 MHz, 128K Cache, 66 MHz FSB	No
1999	Pentium® II 350 MHz, 512K Cache, 100 MHz FSB	No
1999	Pentium® II 400 MHz, 512K Cache, 100 MHz FSB	No
1999	Pentium® II 450 MHz, 512K Cache, 100 MHz FSB	No
1999	Pentium® III 450 MHz, 512K Cache, 100 MHz FSB	Yes
1999	Pentium® III 500 MHz, 256K Cache, 100 MHz FSB	No
1999	Pentium® III 500 MHz, 512K Cache, 100 MHz FSB	No
1999	Pentium® III 533 MHz, 256K Cache, 133 MHz FSB	No
1999	Pentium® III 533 MHz, 512K Cache, 133 MHz FSB	No
1999	Pentium® III 550 MHz, 256K Cache, 100 MHz FSB	No
1999	Pentium® III 550 MHz, 512K Cache, 100 MHz FSB	No
1999	Pentium® III 600 MHz, 256K Cache, 100 MHz FSB	No
1999	Pentium® III 600 MHz, 256K Cache, 133 MHz FSB	No
1999	Pentium® III 600 MHz, 512K Cache, 100 MHz FSB	No
1999	Pentium® III 600 MHz, 512K Cache, 133 MHz FSB	No
1999	Pentium® III 650 MHz, 256K Cache, 100 MHz FSB	Yes
1999	Pentium® III 667 MHz, 256K Cache, 133 MHz FSB	Yes
1999	Pentium® III 700 MHz, 256K Cache, 100 MHz FSB	Yes
1999	Pentium® III 733 MHz, 256K Cache, 133 MHz FSB	Yes
2000	Celeron® 533 MHz, 128K Cache, 66 MHz FSB	No
2000	Celeron® 566 MHz, 128K Cache, 66 MHz FSB	No
2000	Celeron® 600 MHz, 128K Cache, 66 MHz FSB	No
2000	Celeron® 633 MHz, 128K Cache, 66 MHz FSB	No
2000	Celeron® 667 MHz, 128K Cache, 66 MHz FSB	No
2000	Celeron® 700 MHz, 128K Cache, 66 MHz FSB	No
2000	Celeron® 733 MHz, 128K Cache, 66 MHz FSB	No
2000	Celeron® 766 MHz, 128K Cache, 66 MHz FSB	No
2000	Celeron® 800 MHz, 128K Cache, 100 MHz FSB	No
2000	Pentium® 4 1.30 GHz, 256K Cache, 400 MHz FSB	Yes
2000	Pentium® 4 1.40 GHz, 256K Cache, 400 MHz FSB	Yes
2000	Pentium® 4 1.50 GHz, 256K Cache, 400 MHz FSB	Yes
2000	Pentium® III 1.00 GHz, 256K Cache, 133 MHz FSB	Yes
2000	Pentium® III 750 MHz, 256K Cache, 100 MHz FSB	Yes
2000	Pentium® III 800 MHz, 256K Cache, 100 MHz FSB	No
2000	Pentium® III 800 MHz, 256K Cache, 133 MHz FSB	Yes
2000	Pentium® III 850 MHz, 256K Cache, 100 MHz FSB	Yes
2000	Pentium® III 866 MHz, 256K Cache, 133 MHz FSB	Yes
2000	Pentium® III 933 MHz, 256K Cache, 133 MHz FSB	Yes
2001	Celeron® 1.00 GHz, 128K Cache, 100 MHz FSB	No
2001	Celeron® 1.00 GHz, 256K Cache, 100 MHz FSB	No
2001	Celeron® 1.10 GHz, 128K Cache, 100 MHz FSB	No
2001	Celeron® 1.10 GHz, 256K Cache, 100 MHz FSB	No
2001	Celeron® 1.20 GHz, 256K Cache, 100 MHz FSB	No
2001	Celeron® 1.30 GHz, 256K Cache, 100 MHz FSB	No
2001	Celeron® 850 MHz, 128K Cache, 100 MHz FSB	No
2001	Celeron® 900 MHz, 128K Cache, 100 MHz FSB	No
2001	Celeron® 950 MHz, 128K Cache, 100 MHz FSB	No
2001	Pentium® 4 1.60 GHz, 256K Cache, 400 MHz FSB	Yes
2001	Pentium® 4 1.70 GHz, 256K Cache, 400 MHz FSB	Yes
2001	Pentium® 4 1.80 GHz, 256K Cache, 400 MHz FSB	Yes
2001	Pentium® 4 1.90 GHz, 256K Cache, 400 MHz FSB	Yes
2001	Pentium® 4 2.00 GHz, 256K Cache, 400 MHz FSB	Yes
2001	Pentium® 4 2.00 GHz, 512K Cache, 400 MHz FSB	Yes

Entry Year	MPU Description[1]	SPEC Score?
2001	Pentium® 4 2.20 GHz, 512K Cache, 400 MHz FSB	Yes
2001	Pentium® III 1.00 GHz, 256K Cache, 100 MHz FSB	Yes
2001	Pentium® III 1.10 GHz, 256K Cache, 100 MHz FSB	Yes
2001	Pentium® III 1.13 GHz, 256K Cache, 133 MHz FSB	Yes
2001	Pentium® III 1.20 GHz, 256K Cache, 133 MHz FSB	Yes
2002	Celeron® 1.40 GHz, 256K Cache, 100 MHz FSB	No
2002	Celeron® 2.00 GHz, 128K Cache, 400 MHz FSB	No
2002	Celeron® 2.10 GHz, 128K Cache, 400 MHz FSB	No
2002	Pentium® 4 2.26 GHz, 512K Cache, 533 MHz FSB	Yes
2002	Pentium® 4 2.40 GHz, 512K Cache, 400 MHz FSB	Yes
2002	Pentium® 4 2.40 GHz, 512K Cache, 533 MHz FSB	Yes
2002	Pentium® 4 2.50 GHz, 512K Cache, 400 MHz FSB	No
2002	Pentium® 4 2.53 GHz, 512K Cache, 533 MHz FSB	Yes
2002	Pentium® 4 2.60 GHz, 512K Cache, 400 MHz FSB	No
2002	Pentium® 4 2.66 GHz, 512K Cache, 533 MHz FSB	Yes
2002	Pentium® 4 2.80 GHz, 512K Cache, 533 MHz FSB	Yes
2002	Pentium® 4 supporting HT Tech. 3.06 GHz, 512K Cache, 533 MHz FSB	Yes
2003	Celeron® 2.20 GHz, 128K Cache, 400 MHz FSB	No
2003	Celeron® 2.30 GHz, 128K Cache, 400 MHz FSB	No
2003	Celeron® 2.40 GHz, 128K Cache, 400 MHz FSB	No
2003	Celeron® 2.50 GHz, 128K Cache, 400 MHz FSB	No
2003	Celeron® 2.60 GHz, 128K Cache, 400 MHz FSB	No
2003	Celeron® 2.70 GHz, 128K Cache, 400 MHz FSB	No
2003	Celeron® 2.80 GHz, 128K Cache, 400 MHz FSB	No
2003	Pentium® 4 2.80A GHz, 1M Cache, 533 MHz FSB	No
2003	Pentium® 4 supporting HT Tech. 2.40 GHz, 512K Cache, 800 MHz FSB	Yes
2003	Pentium® 4 supporting HT Tech. 2.60 GHz, 512K Cache, 800 MHz FSB	Yes
2003	Pentium® 4 supporting HT Tech. 2.80 GHz, 512K Cache, 800 MHz FSB	Yes
2003	Pentium® 4 supporting HT Tech. 2.80E GHz, 1M Cache, 800 MHz FSB	No
2003	Pentium® 4 supporting HT Tech. 3.00 GHz, 1M Cache, 800 MHz FSB	No
2003	Pentium® 4 supporting HT Tech. 3.00 GHz, 512K Cache, 800 MHz FSB	No
2003	Pentium® 4 supporting HT Tech. 3.20 GHz, 1M Cache, 800 MHz FSB	No
2003	Pentium® 4 supporting HT Tech. 3.20 GHz, 512K Cache, 800 MHz FSB	Yes
2003	Pentium® 4 supporting HT Tech. 3.40 GHz, 1M Cache, 800 MHz FSB	No
2003	Pentium® 4 supporting HT Tech. 3.40 GHz, 512K Cache, 800 MHz FSB	Yes
2003	Pentium® 4 Extreme Ed. supporting HT Tech. 3.20 GHz, 2M Cache, 800 MHz FSB	Yes
2003	Pentium® 4 Extreme Ed. supporting HT Tech. 3.40 GHz, 2M Cache, 800 MHz FSB	Yes
2004	Celeron® D 320 (256K Cache, 2.40 GHz, 533 MHz FSB)	No
2004	Celeron® D 325 (256K Cache, 2.53 GHz, 533 MHz FSB)	No
2004	Celeron® D 330 (256K Cache, 2.66 GHz, 533 MHz FSB)	No
2004	Celeron® D 335 (256K Cache, 2.80 GHz, 533 MHz FSB)	No
2004	Celeron® 2.40 GHz, 256K Cache, 533 MHz FSB	No
2004	Pentium® 4 2.80 GHz, 1M Cache, 533 MHz FSB	Yes
2004	Pentium® 4 530 supporting HT Tech. (1M Cache, 3.00 GHz, 800 MHz FSB)	Yes
2004	Pentium® 4 540 supporting HT Tech. (1M Cache, 3.20 GHz, 800 MHz FSB)	No
2004	Pentium® 4 540J supporting HT Tech. (1M Cache, 3.20 GHz, 800 MHz FSB)	No
2004	Pentium® 4 550 supporting HT Tech. (1M Cache, 3.40 GHz, 800 MHz FSB)	No
2004	Pentium® 4 550J supporting HT Tech. (1M Cache, 3.40 GHz, 800 MHz FSB)	No
2004	Pentium® 4 560 supporting HT Tech. (1M Cache, 3.60 GHz, 800 MHz FSB)	No
2004	Pentium® 4 560J supporting HT Tech. (1M Cache, 3.60 GHz, 800 MHz FSB)	Yes
2004	Pentium® 4 Extreme Ed. supporting HT Tech. 3.46 GHz, 2M Cache, 1066 MHz FSB	Yes
2005	Celeron® D 326 (256K Cache, 2.53 GHz, 533 MHz FSB)	No
2005	Celeron® D 331 (256K Cache, 2.66 GHz, 533 MHz FSB)	No
2005	Celeron® D 336 (256K Cache, 2.80 GHz, 533 MHz FSB)	No
2005	Celeron® D 340 (256K Cache, 2.93 GHz, 533 MHz FSB)	No
2005	Celeron® D 341 (256K Cache, 2.93 GHz, 533 MHz FSB)	No
2005	Celeron® D 345 (256K Cache, 3.06 GHz, 533 MHz FSB)	No
2005	Celeron® D 346 (256K Cache, 3.06 GHz, 533 MHz FSB)	No

Entry Year	MPU Description[1]	SPEC Score?
2005	Celeron® D 350 (256K Cache, 3.20 GHz, 533 MHz FSB)	No
2005	Celeron® D 351 (256K Cache, 3.20 GHz, 533 MHz FSB)	No
2005	Celeron® D 355 (256K Cache, 3.33 GHz, 533 MHz FSB)	No
2005	Pentium® 4 520J supporting HT Tech. (1M Cache, 2.80 GHz, 800 MHz FSB)	No
2005	Pentium® 4 521 supporting HT Tech. (1M Cache, 2.80 GHz, 800 MHz FSB)	Yes
2005	Pentium® 4 530J supporting HT Tech. (1M Cache, 3.00 GHz, 800 MHz FSB)	No
2005	Pentium® 4 531 supporting HT Tech. (1M Cache, 3.00 GHz, 800 MHz FSB)	Yes
2005	Pentium® 4 541 supporting HT Tech. (1M Cache, 3.20 GHz, 800 MHz FSB)	No
2005	Pentium® 4 551 supporting HT Tech. (1M Cache, 3.40 GHz, 800 MHz FSB)	No
2005	Pentium® 4 561 supporting HT Tech. (1M Cache, 3.60 GHz, 800 MHz FSB)	No
2005	Pentium® 4 570J supporting HT Tech. (1M Cache, 3.80 GHz, 800 MHz FSB)	Yes
2005	Pentium® 4 571 supporting HT Tech. (1M Cache, 3.80 GHz, 800 MHz FSB)	No
2005	Pentium® 4 630 supporting HT Tech. (2M Cache, 3.00 GHz, 800 MHz FSB)	Yes
2005	Pentium® 4 631 supporting HT Tech. (2M Cache, 3.00 GHz, 800 MHz FSB)	Yes
2005	Pentium® 4 640 supporting HT Tech. (2M Cache, 3.20 GHz, 800 MHz FSB)	Yes
2005	Pentium® 4 641 supporting HT Tech. (2M Cache, 3.20 GHz, 800 MHz FSB)	No
2005	Pentium® 4 650 supporting HT Tech. (2M Cache, 3.40 GHz, 800 MHz FSB)	Yes
2005	Pentium® 4 651 supporting HT Tech. (2M Cache, 3.40 GHz, 800 MHz FSB)	Yes
2005	Pentium® 4 660 supporting HT Tech. (2M Cache, 3.60 GHz, 800 MHz FSB)	Yes
2005	Pentium® 4 661 supporting HT Tech. (2M Cache, 3.60 GHz, 800 MHz FSB)	No
2005	Pentium® 4 662 supporting HT Tech. (2M Cache, 3.60 GHz, 800 MHz FSB)	No
2005	Pentium® 4 670 supporting HT Tech. (2M Cache, 3.80 GHz, 800 MHz FSB)	Yes
2005	Pentium® 4 672 supporting HT Tech. (2M Cache, 3.80 GHz, 800 MHz FSB)	No
2005	Pentium® D 820 (2M Cache, 2.80 GHz, 800 MHz FSB)	Yes
2005	Pentium® D 830 (2M Cache, 3.00 GHz, 800 MHz FSB)	Yes
2005	Pentium® D 840 (2M Cache, 3.20 GHz, 800 MHz FSB)	Yes
2005	Pentium® D 920 (4M Cache, 2.80 GHz, 800 MHz FSB)	Yes
2005	Pentium® D 930 (4M Cache, 3.00 GHz, 800 MHz FSB)	Yes
2005	Pentium® D 940 (4M Cache, 3.20 GHz, 800 MHz FSB)	Yes
2005	Pentium® D 950 (4M Cache, 3.40 GHz, 800 MHz FSB)	Yes
2005	Pentium® Extreme Ed. 840 (2M Cache, 3.20 GHz, 800 MHz FSB)	Yes
2005	Pentium® Extreme Ed. 955 (4M Cache, 3.46 GHz, 1066 MHz FSB)	Yes
2005	Pentium® 4 Extreme Ed. supporting HT Tech. 3.73 GHz, 2M Cache, 1066 MHz FSB	Yes
2006	Celeron® D 315 (256K Cache, 2.26 GHz, 533 MHz FSB)	No
2006	Celeron® D 347 (512K Cache, 3.06 GHz, 533 MHz FSB)	No
2006	Celeron® D 352 (512K Cache, 3.20 GHz, 533 MHz FSB)	No
2006	Celeron® D 356 (512K Cache, 3.33 GHz, 533 MHz FSB)	No
2006	Core™2 Duo E6300 (2M Cache, 1.86 GHz, 1066 MHz FSB)	Yes
2006	Core™2 Duo E6400 (2M Cache, 2.13 GHz, 1066 MHz FSB)	Yes
2006	Core™2 Duo E6600 (4M Cache, 2.40 GHz, 1066 MHz FSB)	Yes
2006	Core™2 Duo E6700 (4M Cache, 2.66 GHz, 1066 MHz FSB)	Yes
2006	Core™2 Extreme QX6700 (8M Cache, 2.66 GHz, 1066 MHz FSB)	Yes
2006	Core™2 Extreme X6800 (4M Cache, 2.93 GHz, 1066 MHz FSB)	Yes
2006	Pentium® 4 524 supporting HT Tech. (1M Cache, 3.06 GHz, 533 MHz FSB)	No
2006	Pentium® D 805 (2M Cache, 2.66 GHz, 533 MHz FSB)	Yes
2006	Pentium® D 915 (4M Cache, 2.80 GHz, 800 MHz FSB)	No
2006	Pentium® D 925 (4M Cache, 3.00 GHz, 800 MHz FSB)	Yes
2006	Pentium® D 945 (4M Cache, 3.40 GHz, 800 MHz FSB)	Yes
2006	Pentium® D 960 (4M Cache, 3.60 GHz, 800 MHz FSB)	Yes
2006	Pentium® Extreme Ed. 965 (4M Cache, 3.73 GHz, 1066 MHz FSB)	Yes
2007	Celeron® D 365 (512K Cache, 3.60 GHz, 533 MHz FSB)	No
2007	Celeron® 430 (512K Cache, 1.80 GHz, 800 MHz FSB)	No
2007	Celeron® 440 (512K Cache, 2.00 GHz, 800 MHz FSB)	No
2007	Core™2 Duo E4300 (2M Cache, 1.80 GHz, 800 MHz FSB)	Yes
2007	Core™2 Duo E4400 (2M Cache, 2.00 GHz, 800 MHz FSB)	No
2007	Core™2 Duo E4500 (2M Cache, 2.20 GHz, 800 MHz FSB)	Yes
2007	Core™2 Duo E4600 (2M Cache, 2.40 GHz, 800 MHz FSB)	Yes
2007	Core™2 Duo E6320 (4M Cache, 1.86 GHz, 1066 MHz FSB)	No

Entry Year	MPU Description[1]	SPEC Score?
2007	Core™2 Duo E6420 (4M Cache, 2.13 GHz, 1066 MHz FSB)	No
2007	Core™2 Duo E6550 (4M Cache, 2.33 GHz, 1333 MHz FSB)	No
2007	Core™2 Duo E6750 (4M Cache, 2.66 GHz, 1333 MHz FSB)	Yes
2007	Core™2 Duo E6850 (4M Cache, 3.00 GHz, 1333 MHz FSB)	Yes
2007	Core™2 Duo E8190 (6M Cache, 2.66 GHz, 1333 MHz FSB)	No
2007	Core™2 Duo E8200 (6M Cache, 2.66 GHz, 1333 MHz FSB)	Yes
2007	Core™2 Duo E8400 (6M Cache, 3.00 GHz, 1333 MHz FSB)	Yes
2007	Core™2 Duo E8500 (6M Cache, 3.16 GHz, 1333 MHz FSB)	Yes
2007	Core™2 Extreme QX6800 (8M Cache, 2.93 GHz, 1066 MHz FSB)	Yes
2007	Core™2 Extreme QX6850 (8M Cache, 3.00 GHz, 1333 MHz FSB)	Yes
2007	Core™2 Extreme QX9650 (12M Cache, 3.00 GHz, 1333 MHz FSB)	Yes
2007	Core™2 Quad Q6600 (8M Cache, 2.40 GHz, 1066 MHz FSB)	Yes
2007	Core™2 Quad Q6700 (8M Cache, 2.66 GHz, 1066 MHz FSB)	Yes
2007	Core™2 Quad Q9300 (6M Cache, 2.50 GHz, 1333 MHz FSB)	Yes
2007	Core™2 Quad Q9450 (12M Cache, 2.66 GHz, 1333 MHz FSB)	Yes
2007	Core™2 Quad Q9550 (12M Cache, 2.83 GHz, 1333 MHz FSB)	Yes
2007	Pentium® D 935 (4M Cache, 3.20 GHz, 800 MHz FSB)	No
2007	Pentium® E2140 (1M Cache, 1.60 GHz, 800 MHz FSB)	Yes
2007	Pentium® E2160 (1M Cache, 1.80 GHz, 800 MHz FSB)	Yes
2007	Pentium® E2180 (1M Cache, 2.00 GHz, 800 MHz FSB)	No
2007	Pentium® E2200 (1M Cache, 2.20 GHz, 800 MHz FSB)	No
2008	Atom™ 230 (512K Cache, 1.60 GHz, 533 MHz FSB)	No
2008	Celeron® E1200 (512K Cache, 1.60 GHz, 800 MHz FSB)	No
2008	Celeron® E1400 (512K Cache, 2.00 GHz, 800 MHz FSB)	No
2008	Celeron® E1500 (512K Cache, 2.20 GHz, 800 MHz FSB)	No
2008	Core™2 Duo E4700 (2M Cache, 2.60 GHz, 800 MHz FSB)	No
2008	Core™2 Duo E7200 (3M Cache, 2.53 GHz, 1066 MHz FSB)	Yes
2008	Core™2 Duo E7300 (3M Cache, 2.66 GHz, 1066 MHz FSB)	Yes
2008	Core™2 Duo E7400 (3M Cache, 2.80 GHz, 1066 MHz FSB)	Yes
2008	Core™2 Duo E8300 (6M Cache, 2.83 GHz, 1333 MHz FSB)	No
2008	Core™2 Duo E8600 (6M Cache, 3.33 GHz, 1333 MHz FSB)	Yes
2008	Core™2 Extreme QX9770 (12M Cache, 3.20 GHz, 1600 MHz FSB)	Yes
2008	Core™2 Extreme QX9775 (12M Cache, 3.20 GHz, 1600 MHz FSB)	No
2008	Core™2 Quad Q8200 (4M Cache, 2.33 GHz, 1333 MHz FSB)	Yes
2008	Core™2 Quad Q8300 (4M Cache, 2.50 GHz, 1333 MHz FSB)	Yes
2008	Core™2 Quad Q9400 (6M Cache, 2.66 GHz, 1333 MHz FSB)	Yes
2008	Core™2 Quad Q9650 (12M Cache, 3.00 GHz, 1333 MHz FSB)	No
2008	Pentium® E2220 (1M Cache, 2.40 GHz, 800 MHz FSB)	Yes
2008	Pentium® E5200 (2M Cache, 2.50 GHz, 800 MHz FSB)	Yes
2008	Pentium® E5300 (2M Cache, 2.60 GHz, 800 MHz FSB)	Yes
2009	Celeron® E1600 (512K Cache, 2.40 GHz, 800 MHz FSB)	No
2009	Celeron® E3200 (1M Cache, 2.40 GHz, 800 MHz FSB)	No
2009	Celeron® E3300 (1M Cache, 2.50 GHz, 800 MHz FSB)	No
2009	Core™ i3-530 (4M Cache, 2.93 GHz)	Yes
2009	Core™ i3-540 (4M Cache, 3.06 GHz)	Yes
2009	Core™ i5-650 (4M Cache, 3.20 GHz)	Yes
2009	Core™ i5-660 (4M Cache, 3.33 GHz)	Yes
2009	Core™ i5-661 (4M Cache, 3.33 GHz)	Yes
2009	Core™ i5-670 (4M Cache, 3.46 GHz)	Yes
2009	Core™ i5-750 (8M Cache, 2.66 GHz)	Yes
2009	Core™ i7-860 (8M Cache, 2.80 GHz)	Yes
2009	Core™ i7-870 (8M Cache, 2.93 GHz)	Yes
2009	Core™ i7-920 (8M Cache, 2.66 GHz, 4.80 GT/s Intel® QPI)	Yes
2009	Core™ i7-940 (8M Cache, 2.93 GHz, 4.80 GT/s Intel® QPI)	Yes
2009	Core™ i7-950 (8M Cache, 3.06 GHz, 4.80 GT/s Intel® QPI)	Yes
2009	Core™ i7-960 (8M Cache, 3.20 GHz, 4.80 GT/s Intel® QPI)	Yes
2009	Core™ i7-965 Extreme Ed. (8M Cache, 3.20 GHz, 6.40 GT/s Intel® QPI)	Yes
2009	Core™ i7-975 Extreme Ed. (8M Cache, 3.33 GHz, 6.40 GT/s Intel® QPI)	Yes

Entry Year	MPU Description[1]	SPEC Score?
2009	Core™2 Duo E7500 (3M Cache, 2.93 GHz, 1066 MHz FSB)	Yes
2009	Core™2 Duo E7600 (3M Cache, 3.06 GHz, 1066 MHz FSB)	Yes
2009	Core™2 Quad Q8200S (4M Cache, 2.33 GHz, 1333 MHz FSB)	No
2009	Core™2 Quad Q8400 (4M Cache, 2.66 GHz, 1333 MHz FSB)	Yes
2009	Core™2 Quad Q8400S (4M Cache, 2.66 GHz, 1333 MHz FSB)	No
2009	Core™2 Quad Q9400S (6M Cache, 2.66 GHz, 1333 MHz FSB)	No
2009	Core™2 Quad Q9505 (6M Cache, 2.83 GHz, 1333 MHz FSB)	No
2009	Core™2 Quad Q9505S (6M Cache, 2.83 GHz, 1333 MHz FSB)	No
2009	Core™2 Quad Q9550S (12M Cache, 2.83 GHz, 1333 MHz FSB)	No
2009	Pentium® E5400 (2M Cache, 2.70 GHz, 800 MHz FSB)	Yes
2009	Pentium® E6500 (2M Cache, 2.93 GHz, 1066 FSB)	No
2010	Atom™ D410 (512K Cache, 1.66 GHz)	No
2010	Atom™ D425 (512K Cache, 1.80 GHz)	No
2010	Atom™ D510 (1M Cache, 1.66 GHz)	No
2010	Atom™ D525 (1M Cache, 1.80 GHz)	No
2010	Celeron® E3400 (1M Cache, 2.60 GHz, 800 MHz FSB)	No
2010	Celeron® E3500 (1M Cache, 2.70 GHz, 800 MHz FSB)	No
2010	Core™ i3-550 (4M Cache, 3.20 GHz)	Yes
2010	Core™ i3-560 (4M Cache, 3.33 GHz)	Yes
2010	Core™ i5-655K (4M Cache, 3.20 GHz)	No
2010	Core™ i5-680 (4M Cache, 3.60 GHz)	Yes
2010	Core™ i5-750S (8M Cache, 2.40 GHz)	No
2010	Core™ i5-760 (8M Cache, 2.80 GHz)	No
2010	Core™ i7-860S (8M Cache, 2.53 GHz)	No
2010	Core™ i7-870S (8M Cache, 2.66 GHz)	Yes
2010	Core™ i7-875K (8M Cache, 2.93 GHz)	No
2010	Core™ i7-880 (8M Cache, 3.06 GHz)	Yes
2010	Core™ i7-930 (8M Cache, 2.80 GHz, 4.80 GT/s Intel® QPI)	Yes
2010	Core™ i7-970 (12M Cache, 3.20 GHz, 4.80 GT/s Intel® QPI)	No
2010	Core™ i7-980X Extreme Ed. (12M Cache, 3.33 GHz, 6.40 GT/s Intel® QPI)	Yes
2010	Core™2 Quad Q9500 (6M Cache, 2.83 GHz, 1333 MHz FSB)	No
2010	Pentium® E5500 (2M Cache, 2.80 GHz, 800 MHz FSB)	No
2010	Pentium® E5700 (2M Cache, 3.00 GHz, 800 MHz FSB)	No
2010	Pentium® E5800 (2M Cache, 3.20 GHz, 800 MHz FSB)	No
2010	Pentium® E6800 (2M Cache, 3.33 GHz, 1066 FSB)	No
2010	Pentium® G6950 (3M Cache, 2.80 GHz)	Yes
2011	Atom™ D2500 (1M Cache, 1.86 GHz)	No
2011	Atom™ D2700 (1M Cache, 2.13 GHz)	No
2011	Celeron® G440 (1M Cache, 1.60 GHz)	No
2011	Celeron® G460 (1.5M Cache, 1.80 GHz)	No
2011	Celeron® G530 (2M Cache, 2.40 GHz)	No
2011	Celeron® G530T (2M Cache, 2.00 GHz)	No
2011	Core™ i3-2100 (3M Cache, 3.10 GHz)	Yes
2011	Core™ i3-2100T (3M Cache, 2.50 GHz)	Yes
2011	Core™ i3-2105 (3M Cache, 3.10 GHz)	No
2011	Core™ i3-2120 (3M Cache, 3.30 GHz)	Yes
2011	Core™ i3-2120T (3M Cache, 2.60 GHz)	Yes
2011	Core™ i3-2125 (3M Cache, 3.30 GHz)	No
2011	Core™ i3-2130 (3M Cache, 3.40 GHz)	Yes
2011	Core™ i5-2300 (6M Cache, up to 3.10 GHz)	Yes
2011	Core™ i5-2310 (6M Cache, up to 3.20 GHz)	Yes
2011	Core™ i5-2320 (6M Cache, up to 3.30 GHz)	Yes
2011	Core™ i5-2390T (3M Cache, up to 3.50 GHz)	Yes
2011	Core™ i5-2400 (6M Cache, up to 3.40 GHz)	Yes
2011	Core™ i5-2400S (6M Cache, up to 3.30 GHz)	Yes
2011	Core™ i5-2405S (6M Cache, up to 3.30 GHz)	No
2011	Core™ i5-2500 (6M Cache, up to 3.70 GHz)	Yes
2011	Core™ i5-2500K (6M Cache, up to 3.70 GHz)	Yes

Entry Year	MPU Description[1]	SPEC Score?
2011	Core™ i5-2500S (6M Cache, up to 3.70 GHz)	Yes
2011	Core™ i5-2500T (6M Cache, up to 3.30 GHz)	Yes
2011	Core™ i7-2600 (8M Cache, up to 3.80 GHz)	Yes
2011	Core™ i7-2600K (8M Cache, up to 3.80 GHz)	Yes
2011	Core™ i7-2600S (8M Cache, up to 3.80 GHz)	Yes
2011	Core™ i7-2700K (8M Cache, up to 3.90 GHz)	Yes
2011	Core™ i7-3930K (12M Cache, up to 3.80 GHz)	No
2011	Core™ i7-3960X Extreme Ed. (15M Cache, up to 3.90 GHz)	Yes
2011	Core™ i7-980 (12M Cache, 3.33 GHz, 4.8 GT/s Intel® QPI)	No
2011	Core™ i7-990X Extreme Ed. (12M Cache, 3.46 GHz, 6.40 GT/s Intel® QPI)	Yes
2011	Pentium® G620 (3M Cache, 2.60 GHz)	Yes
2011	Pentium® G620T (3M Cache, 2.20 GHz)	Yes
2011	Pentium® G630 (3M Cache, 2.70 GHz)	Yes
2011	Pentium® G630T (3M Cache, 2.30 GHz)	No
2011	Pentium® G6960 (3M Cache, 2.93 GHz)	No
2011	Pentium® G840 (3M Cache, 2.80 GHz)	Yes
2011	Pentium® G850 (3M Cache, 2.90 GHz)	Yes
2011	Pentium® G860 (3M Cache, 3.00 GHz)	Yes
2012	Atom™ D2550 (1M Cache, 1.86 GHz)	No
2012	Celeron® G465 (1.5M Cache, 1.90 GHz)	No
2012	Celeron® G540T (2M Cache, 2.10 GHz)	Yes
2012	Celeron® G550T (2M Cache, 2.20 GHz)	No
2012	Celeron® G555 (2M Cache, 2.70 GHz)	No
2012	Core™ i3-3220 (3M Cache, 3.30 GHz)	Yes
2012	Core™ i3-3220T (3M Cache, 2.80 GHz)	Yes
2012	Core™ i3-3225 (3M Cache, 3.30 GHz)	No
2012	Core™ i3-3240 (3M Cache, 3.40 GHz)	Yes
2012	Core™ i3-3240T (3M Cache, 2.90 GHz)	Yes
2012	Core™ i5-2380P (6M Cache, up to 3.40 GHz)	No
2012	Core™ i5-2450P (6M Cache, up to 3.50 GHz)	No
2012	Core™ i5-2550K (6M Cache, up to 3.80 GHz)	No
2012	Core™ i5-3330 (6M Cache, up to 3.20 GHz)	Yes
2012	Core™ i5-3350P (6M Cache, up to 3.30 GHz)	No
2012	Core™ i5-3450 (6M Cache, up to 3.50 GHz)	Yes
2012	Core™ i5-3450S (6M Cache, up to 3.50 GHz)	No
2012	Core™ i5-3470 (6M Cache, up to 3.60 GHz)	Yes
2012	Core™ i5-3470S (6M Cache, up to 3.60 GHz)	Yes
2012	Core™ i5-3470T (3M Cache, up to 3.60 GHz)	Yes
2012	Core™ i5-3475S (6M Cache, up to 3.60 GHz)	No
2012	Core™ i5-3550 (6M Cache, up to 3.70 GHz)	No
2012	Core™ i5-3550S (6M Cache, up to 3.70 GHz)	No
2012	Core™ i5-3570 (6M Cache, up to 3.80 GHz)	Yes
2012	Core™ i5-3570K (6M Cache, up to 3.80 GHz)	Yes
2012	Core™ i5-3570S (6M Cache, up to 3.80 GHz)	Yes
2012	Core™ i5-3570T (6M Cache, up to 3.30 GHz)	Yes
2012	Core™ i7-3770 (8M Cache, up to 3.90 GHz)	Yes
2012	Core™ i7-3770K (8M Cache, up to 3.90 GHz)	Yes
2012	Core™ i7-3770T (8M Cache, up to 3.70 GHz)	Yes
2012	Core™ i7-3820 (10M Cache, up to 3.80 GHz)	No
2012	Pentium® G2100T (3M Cache, 2.60 GHz)	Yes
2012	Pentium® G2120 (3M Cache, 3.10 GHz)	Yes
2012	Pentium® G640 (3M Cache, 2.80 GHz)	Yes
2012	Pentium® G640T (3M Cache, 2.40 GHz)	Yes
2012	Pentium® G645 (3M Cache, 2.90 GHz)	No
2012	Pentium® G645T (3M Cache, 2.50 GHz)	No
2012	Pentium® G860T (3M Cache, 2.60 GHz)	Yes
2012	Pentium® G870 (3M Cache, 3.10 GHz)	Yes
2013	Celeron® G1620 (2M Cache, 2.70 GHz)	No

Entry Year	MPU Description[1]	SPEC Score?
2013	Celeron® G1620T (2M Cache, 2.40 GHz)	No
2013	Celeron® G1630 (2M Cache, 2.80 GHz)	No
2013	Celeron® G470 (1.5M Cache, 2.00 GHz)	No
2013	Celeron® J1750 (1M Cache, 2.41 GHz)	No
2013	Celeron® J1850 (2M Cache, 2.00 GHz)	No
2013	Core™ i3-3210 (3M Cache, 3.20 GHz)	No
2013	Core™ i3-3245 (3M Cache, 3.40 GHz)	No
2013	Core™ i3-3250 (3M Cache, 3.50 GHz)	No
2013	Core™ i3-3250T (3M Cache, 3.00 GHz)	No
2013	Core™ i3-4130 (3M Cache, 3.40 GHz)	No
2013	Core™ i3-4130T (3M Cache, 2.90 GHz)	No
2013	Core™ i3-4330 (4M Cache, 3.50 GHz)	Yes
2013	Core™ i3-4330T (4M Cache, 3.00 GHz)	No
2013	Core™ i3-4340 (4M Cache, 3.60 GHz)	No
2013	Core™ i5-3340 (6M Cache, up to 3.30 GHz)	No
2013	Core™ i5-3340S (6M Cache, up to 3.30 GHz)	No
2013	Core™ i5-4430 (6M Cache, up to 3.20 GHz)	Yes
2013	Core™ i5-4430S (6M Cache, up to 3.20 GHz)	No
2013	Core™ i5-4440 (6M Cache, up to 3.30 GHz)	No
2013	Core™ i5-4440S (6M Cache, up to 3.30 GHz)	No
2013	Core™ i5-4570 (6M Cache, up to 3.60 GHz)	Yes
2013	Core™ i5-4570S (6M Cache, up to 3.60 GHz)	No
2013	Core™ i5-4570T (4M Cache, up to 3.60 GHz)	No
2013	Core™ i5-4670 (6M Cache, up to 3.80 GHz)	No
2013	Core™ i5-4670K (6M Cache, up to 3.80 GHz)	Yes
2013	Core™ i5-4670S (6M Cache, up to 3.80 GHz)	No
2013	Core™ i5-4670T (6M Cache, up to 3.30 GHz)	No
2013	Core™ i7-3970X Extreme Ed. (15M Cache, up to 4.00 GHz)	No
2013	Core™ i7-4765T (8M Cache, up to 3.00 GHz)	No
2013	Core™ i7-4770 (8M Cache, up to 3.90 GHz)	Yes
2013	Core™ i7-4770K (8M Cache, up to 3.90 GHz)	No
2013	Core™ i7-4770R (6M Cache, up to 3.90 GHz)	No
2013	Core™ i7-4770S (8M Cache, up to 3.90 GHz)	No
2013	Core™ i7-4770T (8M Cache, up to 3.70 GHz)	No
2013	Core™ i7-4771 (8M Cache, up to 3.90 GHz)	No
2013	Pentium® G2010 (3M Cache, 2.80 GHz)	No
2013	Pentium® G2020 (3M Cache, 2.90 GHz)	Yes
2013	Pentium® G2020T (3M Cache, 2.50 GHz)	No
2013	Pentium® G2030 (3M Cache, 3.00 GHz)	No
2013	Pentium® G2030T (3M Cache, 2.60 GHz)	No
2013	Pentium® G2120T (3M Cache, 2.70 GHz)	No
2013	Pentium® G2130 (3M Cache, 3.20 GHz)	Yes
2013	Pentium® G2140 (3M Cache, 3.30 GHz)	No
2013	Pentium® G3220 (3M Cache, 3.00 GHz)	Yes
2013	Pentium® G3220T (3M Cache, 2.60 GHz)	No
2013	Pentium® G3240T (3M Cache, 2.70 GHz)	No
2013	Pentium® G3420 (3M Cache, 3.20 GHz)	Yes
2013	Pentium® G3430 (3M Cache, 3.30 GHz)	No
2013	Pentium® J2850 (2M Cache, 2.41 GHz)	No

1. MPU description is identical to that on Intel's ARK database except for the following changes to save space: "Intel®" at beginning of description has been omitted, "Processor" has been omitted, and "Edition" and "Technology" have been abbreviated to "Ed." and "Tech." respectively.

Appendix C: Regression Results Using MPU Characteristics

Introduction period only, 2000-06

	2000-01	2001-02	2002-03	2003-04	2004-05	2005-06
Year dummy	-1.227** (.242)	-.465 (.304)	-.561** (.168)	-.093 (.283)	-.092 (.143)	-.155 (.351)
ln *Clock speed*	5.28* (1.88)	3.05 (2.17)	5.28* (1.99)	3.53 (1.74)	4.35** (1.06)	2.73 (1.80)
ln *Power*	-3.19* (1.24)	-1.10 (1.61)	-2.50 (1.95)	-.29 (1.62)	.69 (.66)	-.19 (1.18)
Number of cores					.31 (.28)	.50 (.55)
Number of threads						
ln *Lithography*	2.45* (1.02)	.54 (1.32)		2.51* (.68)	1.22** (.36)	.29 (1.16)
ln *Cache*	-.70 (.64)	-.73 (.59)	.28* (.09)	.19* (.07)	.39* (.17)	.17 (.58)
GPU dummy						
Number of Obs.	20	18	14	11	24	31
Adjusted R^2	.64	.56	.81	.91	.88	.26

Full sample, 2000-06

	2000-01	2001-02	2002-03	2003-04	2004-05	2005-06
Year dummy	-.928** (.097)	-.427** (.070)	-.422** (.082)	-.378** (.056)	-.140* (.062)	-.275** (.087)
ln *Clock speed*	3.14** (.76)	2.71** (.55)	2.08** (.63)	2.12** (.70)	4.16** (.49)	3.41** (.58)
ln *Power*	-1.55** (.54)	-1.47** (.40)	-1.08* (.54)	.77 (.60)	.39 (.33)	-.24 (.37)
Number of cores					.55** (.12)	.57** (.14)
Number of threads						
ln *Lithography*	.94 (.75)	.69 (.46)	1.33 (.71)	2.65** (.23)	1.99** (.16)	1.09** (.30)
ln *Cache*	-.27 (.50)	-.36 (.24)	.34** (.07)	.27** (.03)	.26** (.02)	.26** (.07)
GPU dummy						
Number of Obs.	100	111	94	78	110	168
Adjusted R^2	.51	.54	.56	.91	.88	.49

Introduction period only, 2006-13

	2006-07	2007-08	2008-09	2009-10	2010-11	2011-12	2012-13
Year dummy	-.286 (.302)	.183 (.114)	-.460** (.134)	-.115 (.091)	-.228* (.083)	-.353** (.063)	-.060 (.073)
ln *Clock speed*	.02 (1.45)	.02 (.42)	4.34** (.75)	5.05** (.59)	2.86** (.39)	2.04** (.29)	2.02** (.51)
ln *Power*	.54 (.98)	2.53** (.39)	.93* (.44)	-.24 (.34)	-1.22** (.17)	-.89** (.13)	-.80** (.25)
Number of cores	.11 (.43)	-.38** (.11)	.29 (.15)	.61** (.18)	.37** (.11)	.38** (.09)	.39** (.14)
Number of threads			.03 (.03)	.11* (.04)	.02 (.03)	.08** (.02)	.09** (.03)
ln *Lithography*	1.08 (.91)	1.37** (.39)	.56 (.79)	3.73** (1.08)	.41 (.50)	-.33 (.19)	-.15 (.30)
ln *Cache*	.87 (.56)	.85** (.15)	.10 (.22)	-.42 (.39)	.44 (.36)	.15 (.25)	.15 (.35)
GPU dummy			-.03 (.30)	1.03* (.46)	-.41 (.22)	-.24 (.15)	
Observations	29	29	30	27	35	50	32
Adjusted R^2	.60	.96	.93	.94	.97	.97	.93

Full sample, 2006-13

	2006-07	2007-08	2008-09	2009-10	2010-11	2011-12	2012-13
Year dummy	-.414** (.132)	-.271** (.086)	-.348** (.060)	-.148** (.038)	-.161** (.033)	-.188** (.026)	-.028 (.022)
ln *Clock speed*	1.59* (.62)	.47 (.42)	1.14** (.31)	2.08** (.26)	2.10** (.21)	2.36** (.17)	2.21** (.17)
ln *Power*	-.43 (.40)	-.49 (.34)	.09 (.27)	-.53* (.19)	-.63** (.09)	-.90** (.08)	-.96** (.08)
Number of cores	.55* (.18)	.43** (.12)	.25** (.08)	.33** (.06)	.22** (.04)	.28** (.03)	.47** (.05)
Number of threads			.07** (.02)	.09** (.01)	.07** (.01)	.07** (.01)	.10** (.01)
ln *Lithography*	.86 (.44)	.71* (.28)	.38 (.20)	.37 (.20)	-.43* (.17)	.13 (.10)	.41** (.08)
ln *Cache*	.35 (.24)	.64** (.13)	.47** (.08)	.36** (.06)	.44** (.07)	.44** (.07)	-.03 (.15)
GPU dummy			.13 (.18)	.06 (.10)	-.36** (.07)	-.23** (.04)	-.13 (.08)
Observations	162	170	209	236	291	296	217
Adjusted R^2	.44	.67	.76	.85	.87	.91	.95

Note: The dependent variable is ln(MPU price); the regressions include a constant, not shown above. Standard errors are in parentheses. * and ** indicate significance at the 5% and 1% levels, respectively. An omitted coefficient indicates there was no variation in that variable across models.